February 2010

Application Note

AN-EVAL 2x8-ISO1H812G-1

Coreless Transformer Isolated
High Side Switch Evaluation Board
2 x 8 Channel 0.6A with ISO1H812G

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Power Management & Drives

Never stop thinking

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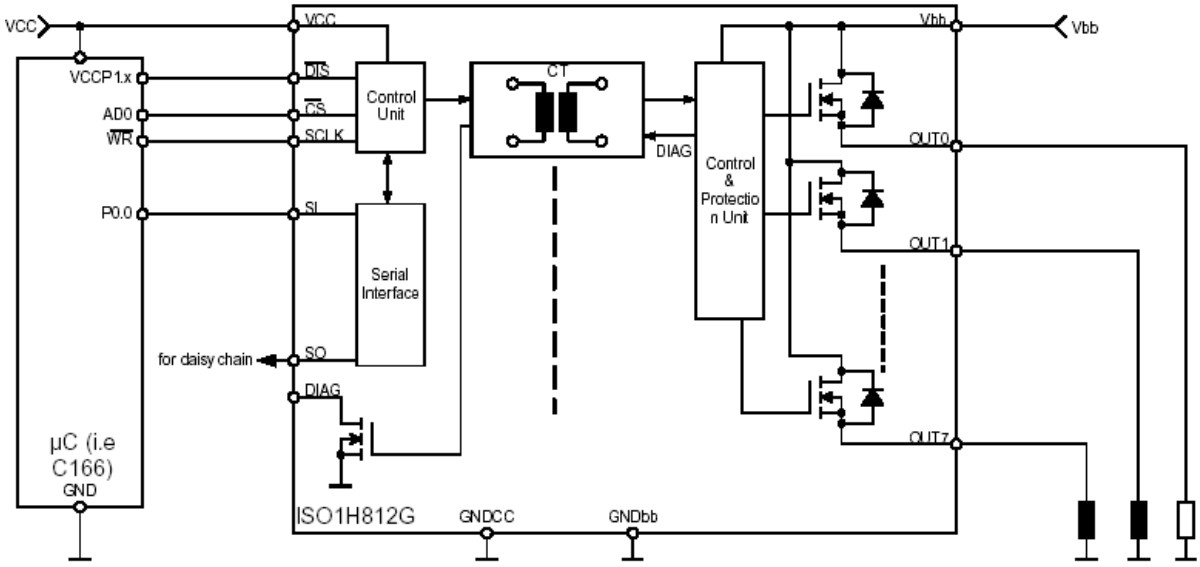
Introduction

Application

This Application Note describes a Demoboard with an isolated 2 x 8 Channel 0.6A Digital Output. The board is designed to show the performance of the ISOFACE® Part **ISO1H812G** providing an Isolated Interface output to drive resistive, capacitive or inductive loads directly. The input can be driven by applying 3,3V/5V CMOS compatible signals to connector K3. The input operates in Micro Controller Mode by using Chip Select and SCLK Signals. The Output consists of 2 times 8 Channel High Side Switches with 0.6A Current rating. The Output is protected with a channel selected over-temperature switch (to off).



Typical Application

ISO1H812G

The **ISO1H812G** is a galvanic isolated 8-bit data interface in P-DSO-36 package that provides 8 fully protected high-side power switches that are able to handle currents up to 625 mA.

An SPI microcontroller (µC) compatible interface allows connecting the IC directly to a µC system. The input interface is designed to operate with 3,3V/5V CMOS compatible levels. The data transfer from input to output side is realized by the integrated Coreless Transformer Technology.

This device includes 8 high-side power switches that are controlled by means of the integrated serial interface. The interface is 8-bit µC compatible. The ISOFACE® can replace optocouplers and the 8 high-side switches in conventional I/O-Applications as galvanic isolation is implemented by means of the integrated coreless transformer technology. The µC compatible interface allows a direct connection to the ports of a microcontroller without the need for other components. Each of the 8 high-side power switches is protected against short to Vbb, overload, over-temperature and against over-voltage by an active zener clamp.

The diagnostic logic on the power chip recognizes the over-temperature information of each power transistor. That information is sent via the internal coreless transformer to the pin DIAG at the input interface.

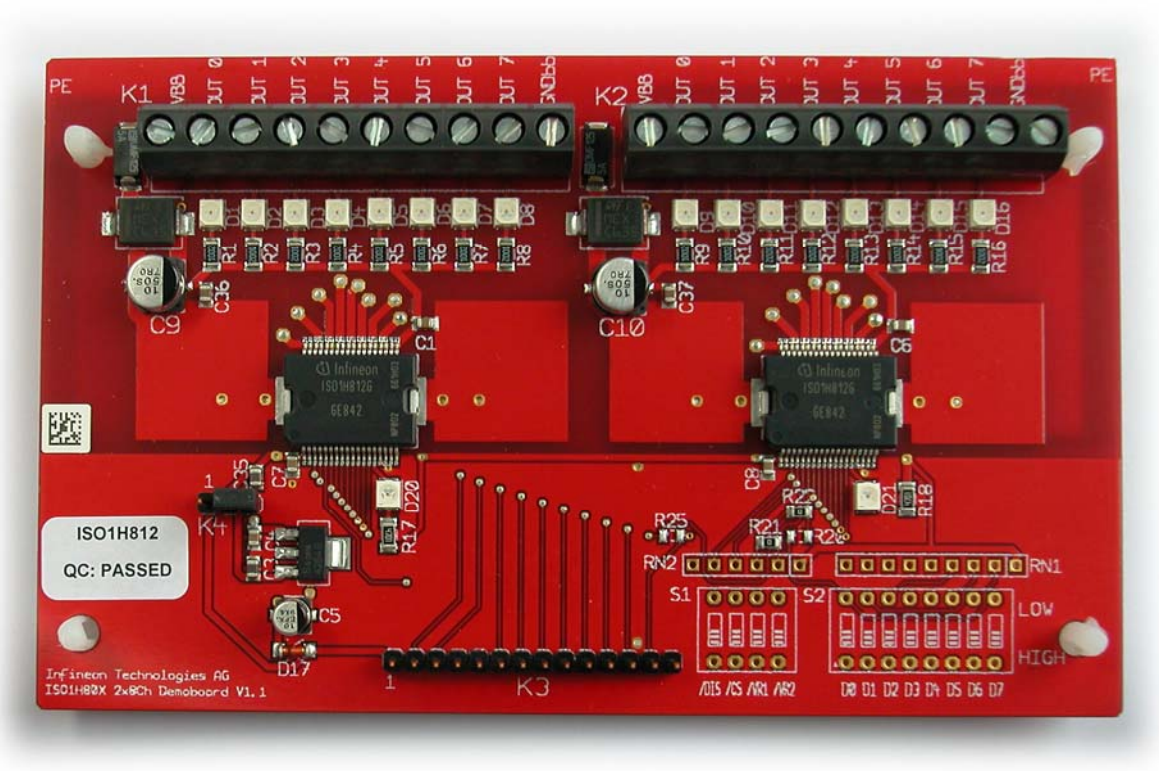


Figure 1– EVAL 2x8-ISO1H812G

Board Characteristics

Parameter	Min.	Max	Unit	Remarks
VCC Input Voltage	3.0	5.5	V	K4 Jumper 1-2
	8	12	V	K4 Jumper 2-3
VBB Input Voltage	11	45	V	
Input Signals	-0.3	0.3xVCC	V	low level
	0.7xVCC	VCC+0.3V	V	high level
Output Current Limit	0.7	1.9	A	
Output Clamping Voltage	47	60	V	

Functional Description

Power Supply

The Demo Board contains 2 galvanic isolated voltage domains that are independent from each other. The input interface is supplied by Pin1 and Pin14 of K3.

Jumper K4 selects direct supply from K3 Pin1 either with 3,3V/5V VCC (Jumper 1-2) or using the on-board 5V voltage regulator (Jumper 2-3). The output stage is supplied at pin1 and 10 of K2, and K2 with Vbb voltage. The different voltage domains can be switched on at different times. The output stage is only enabled once the input stage enters a stable state.

Serial Interface

The ISO1H812G contains a serial interface that can be directly controlled by the microcontroller output ports.

SPI Signal Description

CS - Chip select. The system microcontroller selects the ISO1H812G by means of the CS pin. Whenever the pin is in a logic low state, data can be transferred from the µC.

CS High-to-low transition:

- Serial input data can be clocked in from then on
- SO changes from high impedance state to logic high or low state corresponding to the SO bit-state

CS Low-to-high transition:

- Transfer of SI bits from shift register into output buffers, if number of clock signals was an integer multiple of 8
- SO changes from the SO bit-state to high impedance state

To avoid any false clocking, the serial input pin SCLK should be logic high state during high-to-low transition of CS. When CS is in a logic high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state. The integrated modulo counter that counts the number of clocks avoids the take over of invalid commands caused by a spike on the clock line or wrong number of clock cycles. A command is only taken over after the low-to-high transition of the CS signal, if the number of counted clock cycles is an integer multiple of 8.

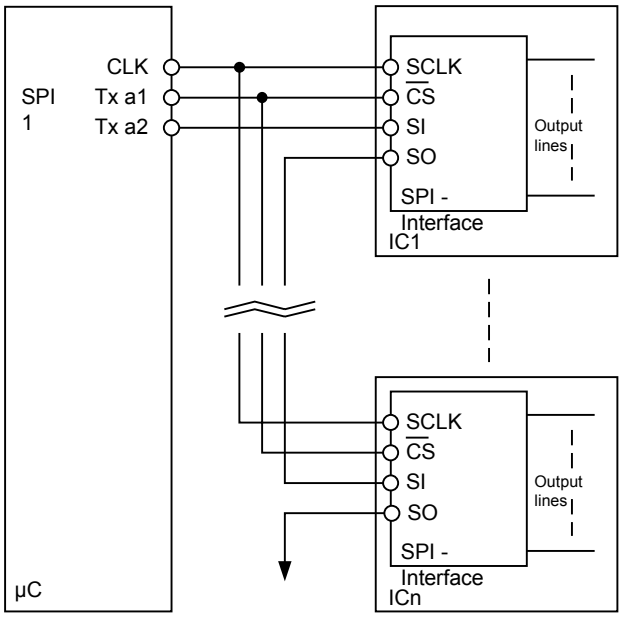
SCLK - Serial clock. The system clock pin clocks the internal shift register of the ISO1H812G. The serial input (SI) accepts data into the input shift register on the rising edge of SCLK while the serial output (SO) shifts the output information out of the shift register on the falling edge of the serial clock. It is essential that the SCLK pin is in a logic high state whenever chip select /CS makes any transition. The number of clock pulses will be counted during a chip select cycle. The received data will only be accepted, if exactly an integer multiple of 8 clock pulses were counted during CS is active.

SI - Serial input. Serial data bits are shifted in at this pin, the most significant bit first. SI information is read in on the rising edge of the SCLK. Input data is latched in the shift register and then transferred to the control buffer of the output stages.

SO - Serial output. SO is in a high impedance state until the CS pin goes to a logic low state. The data of the internal shift register are shifted out serially at this pin. The most significant bit will appear at first. The further bits will appear following the falling edge of SCLK.

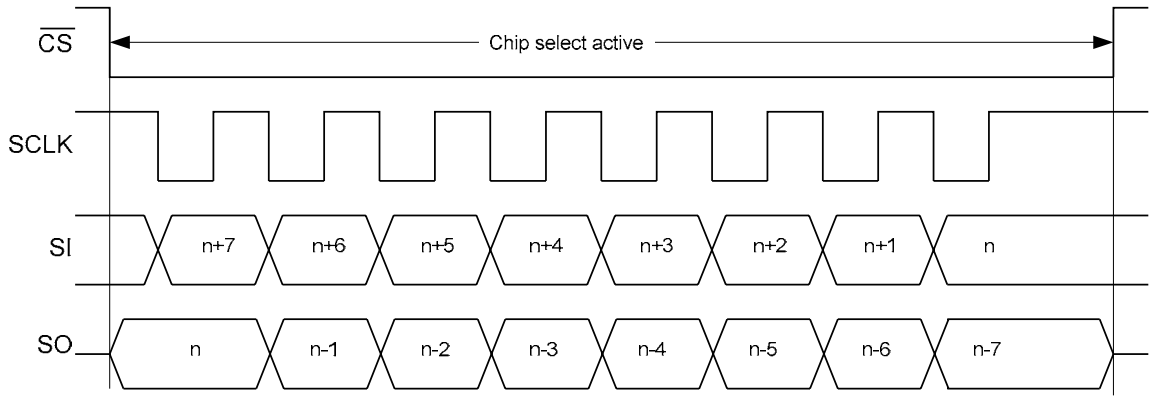
Daisy-chain Configuration

the connection of different ICs and a µC as shown below is called a daisy-chain. For this type of bus-topology only one SPI interface of the µC for two or more ICs is needed. All ICs share the same clock and chip select port of the SPI master. That is all ICs are active and addressed simultaneously. The data out of the µC is connected to the SI of the first IC in the line. Each SO of an IC is connected to the SI of the next IC in the line.



Number of adressed ICs = n
Number of necessary control and data ports = 3
All ICs are adressed by the common chip select

SPI 8 Bit Transfer Signal Timing



Output Stage

Each channel contains a high-side vertical power FET that is protected by embedded protection functions. The continuous current for each channel is 625mA (all channels ON).

Each output is independently controlled by an output latch and a common reset line via the pin /DIS that disables all eight outputs and reset the latches. A logic high input data bit turns the respective output channel ON. A logic low data bit turns that output channel OFF.

Power Transistor Over-Voltage Protection

Each of the eight output stages has it own zener clamp that causes a voltage limitation at the power transistor when inductive loads are switched off. V_{ON} is then clamped to 47V (min.).

Inductive and over-voltage output clamp (each channel)

Energy is stored in the load inductance.

$$E_L = 1 / 2 \times L \times I_L^2$$

Inductive load switch-off energy dissipation (each channel)

While demagnetizing the load inductance, the energy dissipation in the DMOS with an approximate solution for $R_L > 0\Omega$ is:

$$E_{AS} = \frac{I_L \times L}{2 \times R_L} \times (V_{bb} + |V_{ON(CL)}|) \times \ln\left(1 + \frac{I_L \times R_L}{|V_{ON(CL)}|}\right)$$

Power Transistor Over-current Protection

The outputs are provided with a current limitation that enters a repetitive switched mode after an initial peak current has been exceeded. The initial peak short circuit current limit $I_{L(SCp)}$ is set to a minimum of 0.7A at T_j = 125°C. During the repetitive mode, short circuit current limit $I_{L(SCr)}$ is set to 1.1A (typ.). If this operation leads to an over-temperature condition, a second protection level (T_j > 135°C) will change the output into a low Pulse-Width Modulated duty cycle (selective thermal shutdown with restart) to prevent critical chip temperatures.

Common Diagnostic Output

The over-temperature detection information of the channels is OR-wired in the common diagnostic output block. The information is send via the integrated coreless transformer to the input interface. The output stage at pin DIAG has an open drain functionality combined with a current source. The red LED D20 and D21 show the current state of the DIAG output.

LED ON: one of the Channels has over-temperature or the VBB Supply is below the operating range

Connectors

K1, K2:

	K1	K2
1	VBB1	VBB2
2	OUT10	OUT20
3	OUT11	OUT21
4	OUT12	OUT22
5	OUT13	OUT23
6	OUT14	OUT24
7	OUT15	OUT25
8	OUT16	OUT26
9	OUT17	OUT27
10	GNDbb1	GNDbb2

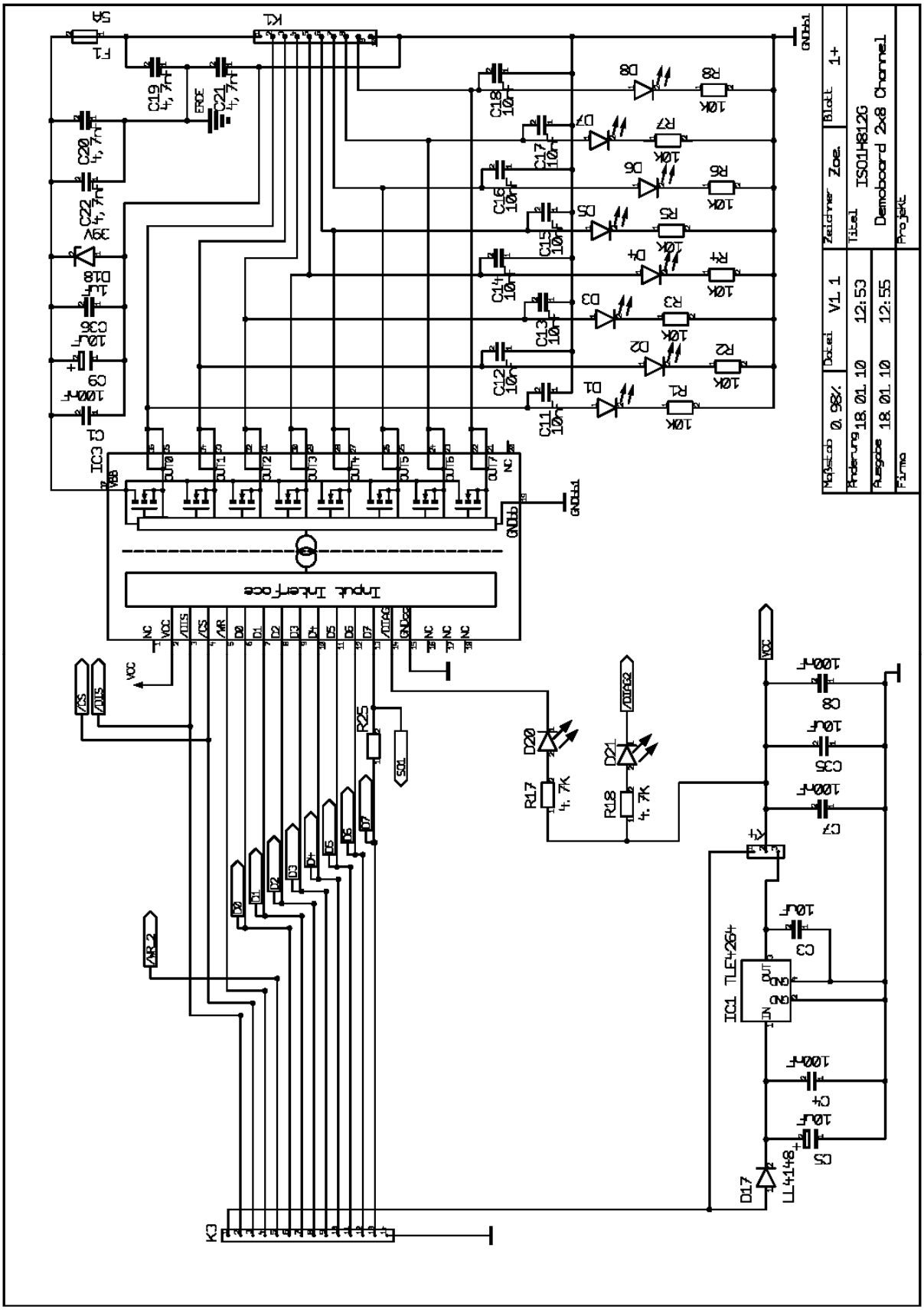
K3:

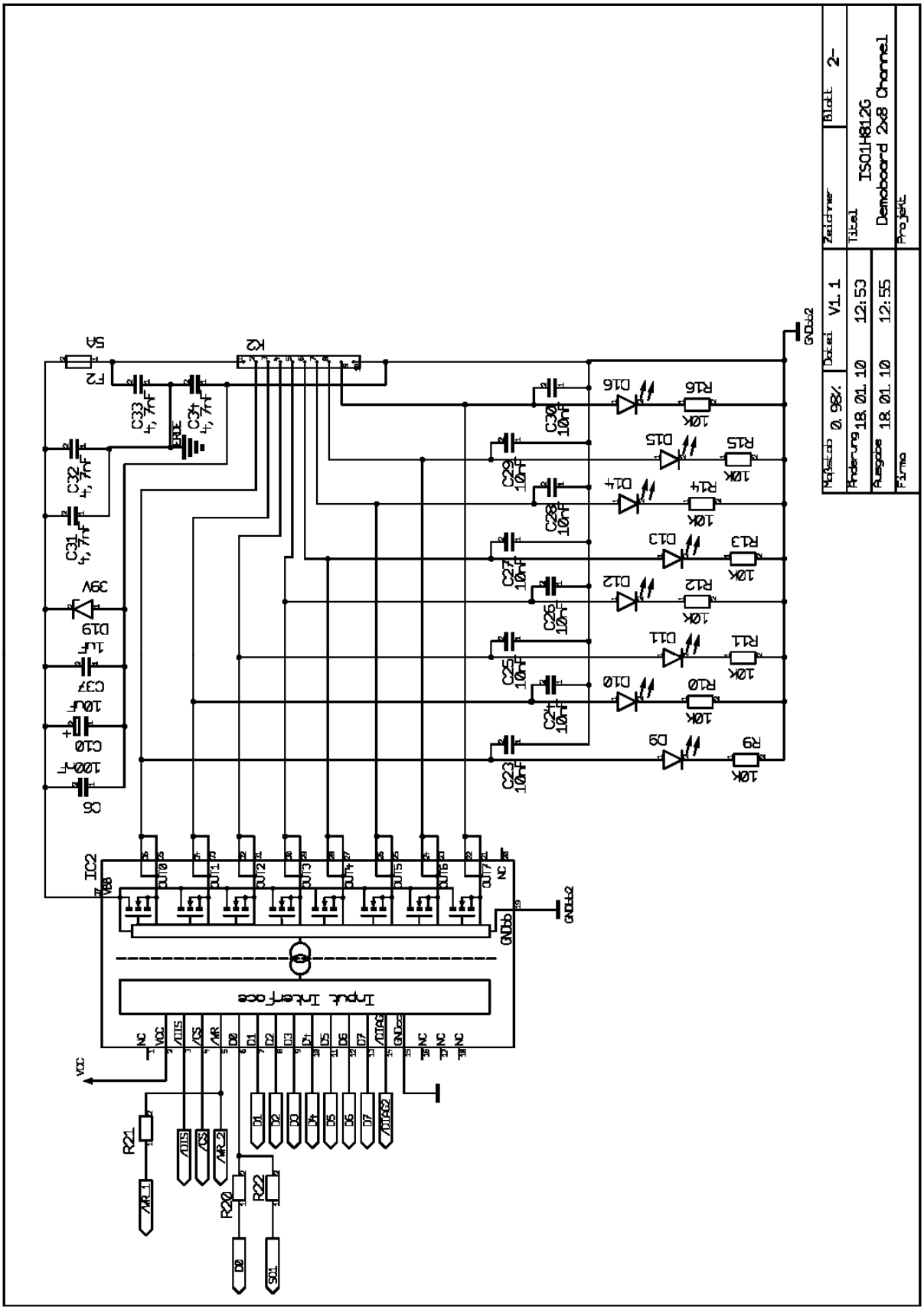
1	+Vin/VCC
2	/DIS
3	/CS
4	SCLK
5	
6	SI
7	
8	
9	
10	
11	
12	
13	SO
14	GNDCC

K4:

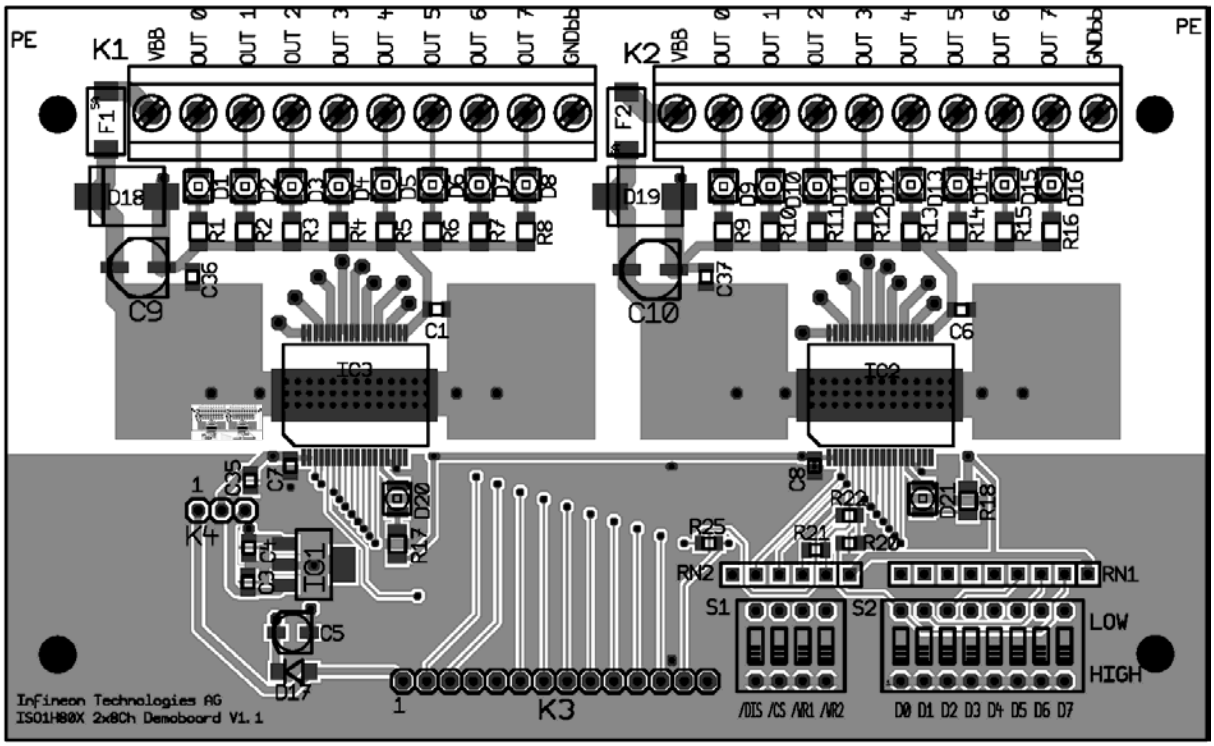
Jumper 1 - 2	VCC 3,3V/5V
Jumper 2 - 3	Vin 8V …12V

Schematic

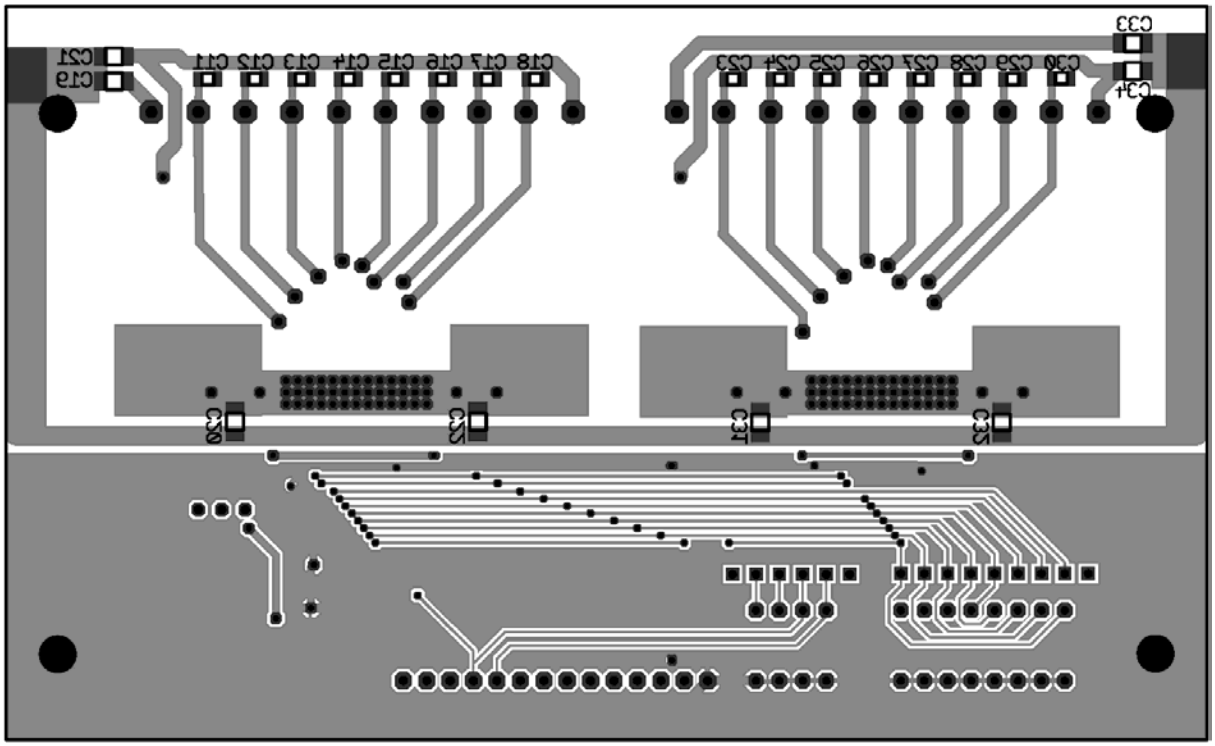

Input Interface
IC1 TLE4264
D17 LL4148
Titel ISO1H812G Demoboard 2x8 Channel
Zeichner Zoe.
Datei V1.1
Änderung 18.01.10 12:53
Ausgabe 18.01.10 12:55
Firma
Projekt
Blatt 1+


ISO1H812G
Demoboard 2x8 Channel
Input Interface

PCB Layout and Assembly



Board Layout - Component Side



Board Layout - Bottom Side (mirror view)

Bill of Material

Nr.	Quant.	Position	Value	Package
1	5	C1, C4, C6, C7, C8	100nF, 50V	0805
2	2	C36, C37	1uF, 50V	0805
3	2	C9, C10	10uF, 50V	SMD_E
4	2	C3, C35	10uF, 10V	0805
4	16	C11, C12, C13, C14, C15, C16, C17, C18, C23, C24, C25, C26, C27, C28, C29, C30	10nF, 50V	0805
5	8	C19, C20, C21, C22, C31, C32, C33, C34	4,7nF, 500V	1206
6	1	C5	10uF, 25V	SMD_B
7	16	D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16	LED gn	P-LCC-2
8	2	D20, D21	LED rt	P-LCC-2
9	1	D17	LL4148	MM
10	2	D18, D19	SM15T39A	SMC
11	2	F1, F2	OMF125, 5A	SMD-D/E
12	1	IC1	TLE4264	SOT-223
13	2	IC2, IC3	ISO1H812G	P-DSO36
14	2	K1, K2	Terminal 10pol.	RM5,08
15	1	K3	Connector 14pol.	RM2,54
16	1	K4	Connector 3pol.	RM2,54
17	16	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16	10k	1206
18	2	R17, R18	4,7k	1206
19	2	R21, R22	0R	805
20	1	K4	Jumper	
21	4		Spacer	
22	1		Print Board	

References

[1] ISO1H812G Coreless Transformer Isolated Digital Output 8 Channel 0.625A High Side Switch, Data Sheet, Infineon Technologies

Change service

Revision History			
Application Note EVAL2x8-ISO1H812G-1			
Actual Release: V1.1	Date: 15.02.2010		Previous Release:
Page of actual Rel.	Page of prev. Rel.	Subjects changed since last release	
11	----------	First Issue	

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