Zipper and Myriad-RF Development Kit Manual

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Introduction

The Zipper and Myriad RF boards' combination is a low cost universal radio development platform, based on flexible, multi standard LMS6002D**.** It enables developers to implement their products for a wide variety of wireless communication applications efficiently. The main ideas are to:

- Make use of a ready-made design and implementation to accelerate the development time.
- Experiment and evaluate new modulation schemes and wireless systems, operating over a wide frequency range.
- Easily modify and manufacture the platform for new designs using the Open Source database for the complete Kit.

This document provides the following information:

- Detailed description of the hardware platform including setup.
- Software installation, setup and programming of the LMS6002DFN.
- Example files for running the complete platform.

2

Development System Contents

Fully operational development system contains Myriad-RF board, Zipper board and Zipper software. See Figure 1. Zipper and Myriad-RF board development system below.

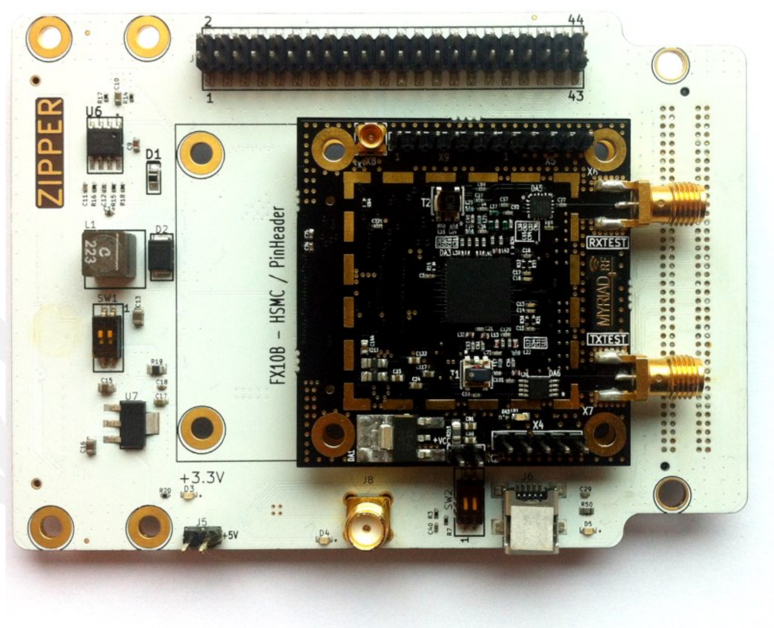


Figure 1. Zipper and Myriad-RF board development system

The universal interface board (Zipper board) allows user to connect to every available baseband to Myriad RF board and start developing new applications for RF communication see Figure 2. On top of that, the board provides the flexibility to select desired digital interface frequency and synchronize to reduce frequency error.

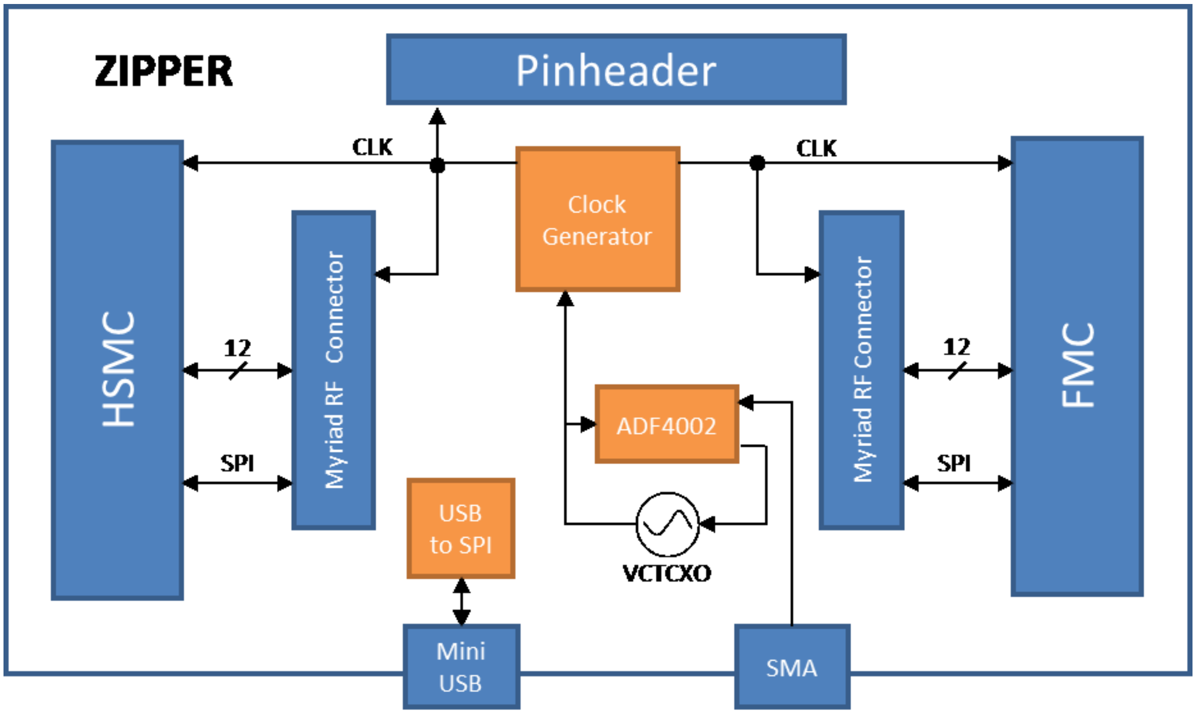


Figure 2. Zipper board block diagram.

3

Installing and Running the Software Application

3.1 Windows XP Operating System

Communications through the USB port have become a standard feature on almost every new personal computer. Zipper board contains the USB to SPI interface converter and together with PC software application allows user simplified control of Myriad RF board.

As for every new USB device plug in to your PC the USB drivers have to be installed. Before plugging the USB cable to USB port, make sure that you are logged in as Administrator.

When the device is plugged in the USB connector the following Wizard window comes up.

Figure 3. Hardware wizard

Select “No, not this time option and click on Next

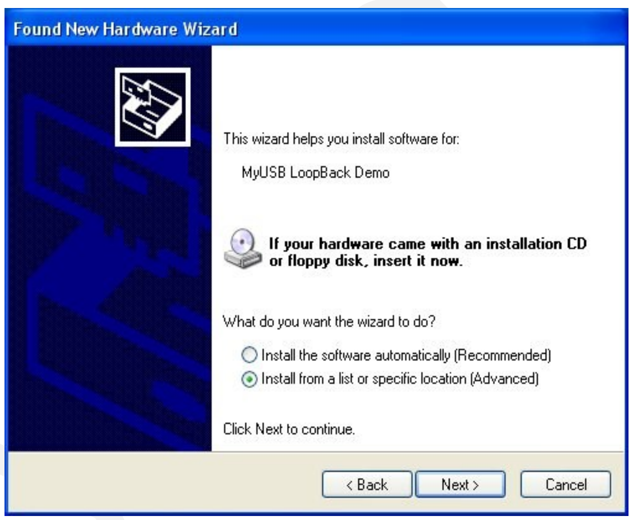


Figure 4. Install driver manually

Select “Install from a list or specific location (Advanced)” option and click on Next.

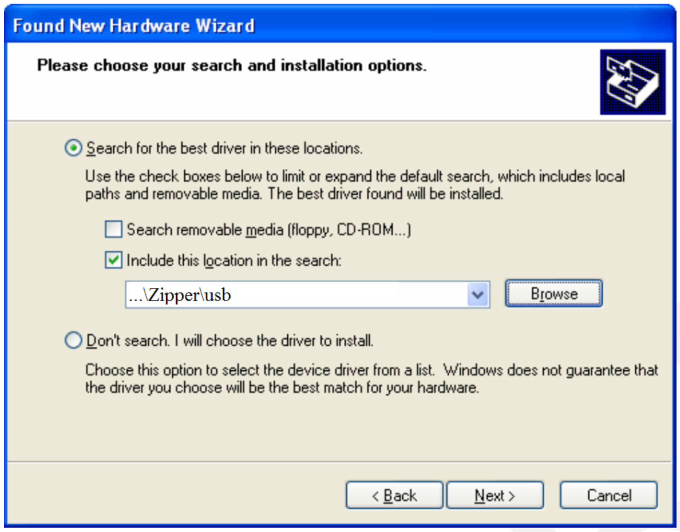


Figure 5. Choose the USBDriver.inf from the folder

Select "Search for the best driver in these locations" option, then select "Include this location in the search" and check if the following path is correctly setup : <your_HDD>:\ <your_path>\ Zipper\usb.

Windows should proceed to install drivers. Enumeration process (USB term meaning *"connect and establish communication with"*) should start now. If everything is successful unplug and then plug in your device again to be able to use it.

3.2 Determining Serial Ports

After installation Windows will assign to your USB Virtual Serial device a serial port.

To check the serial port number, please use the following procedure:

1. Right-Click on **My Computer**.
2. Click **Properties** and select the **Hardware** tab.
3. Select **Device Manager.** New widow has to open. Find **USB Virtual Serial Port** under "Ports (COM & LPT)". Note that in this system example it has enumerated as COM3 .

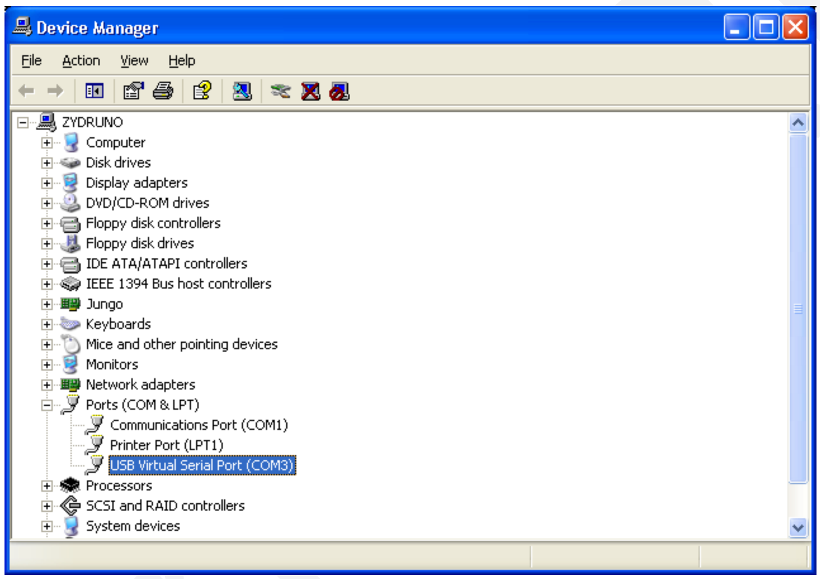


Figure 6. Check in device manager the new communication port

3.3 Windows 7 Operating System

Plug USB cable to USB port of the interface board. No external power connection is required.

After plugging in the board the USB driver needs to be installed. To install the USB driver do the following:

1. Click on Control Panel ⟶ System and Security ⟶ System.
2. Click on Device Manager ⟶ other devices.
3. Right click on "LUFA USB-RS232 Demo" icon.
4. Click on Update Driver Software and select 2nd option: Browse my computer for driver software. Locate and install driver software manually as shown below.

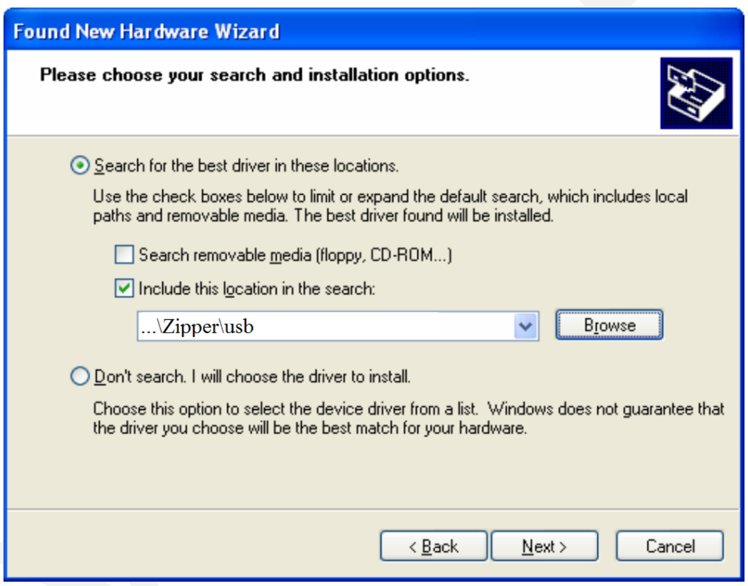


Figure 7. Choose the USBDriver.inf from the folder.

5. The folder should point to the `USBDriver.inf` file, which can be found in the **Zipper** folder. Use the browse function to find this file.
6. Windows should proceed to install drivers. Enumeration process (USB term meaning *"connect and establish communication with"*) should start now. If everything is successful unplug and then plug in your device again to be able to use it.

To determine the assign port number you follow procedure described in section *"3.2 Determining serial ports"*.

3.4 Using Zipper Software

This section describes how to set up Zipper software tool and communication with Zipper board. The Zipper software is shown below.

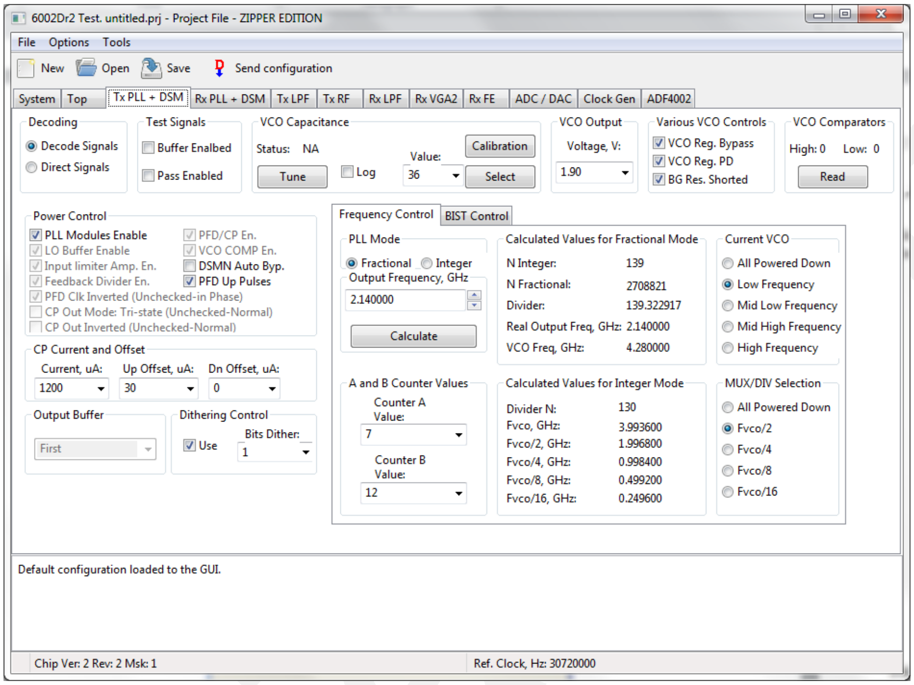


Figure 8. Zipper software main window.

3.4.1. Assign COM port and perform register test

Connect the board to your PC and start the application. Go to menu "Options->Communication Settings". The following window appears

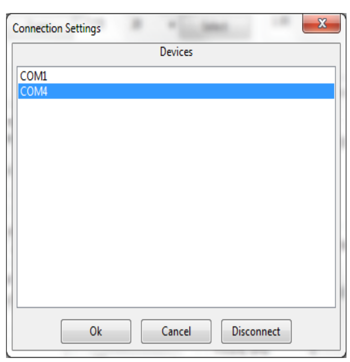


Figure 9. Zipoper software Comunication settings.

Select enumerated port under USB board. In this example COM port number is 4, but port number can be different in another case.

To check if communication with Myriad RF board is functioning, select the register test sequence by going to menu “Tools->Register Test”.

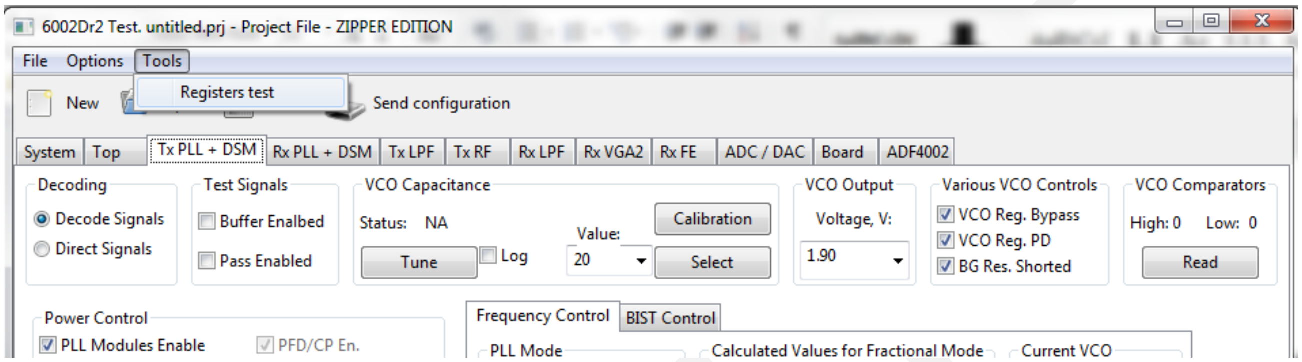


Figure 10. Zipoper software Register Test.

The system will then return a full registers indicating OK for correct operation as shown below.

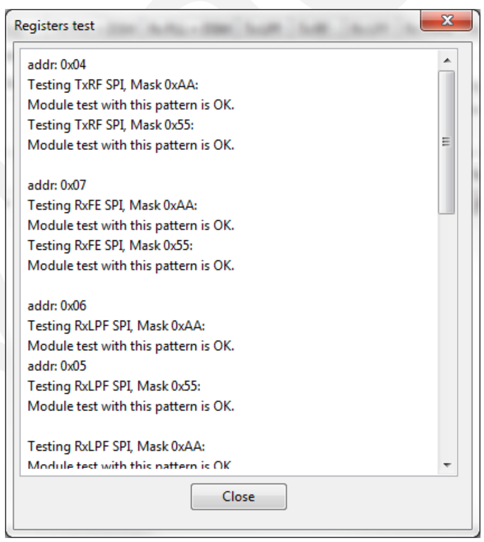


Figure 11. Zipoper software Register Test Log.

If the system returns OK message you are now ready to commence testing. If the system returns 00 or FF instead of the OK this means there is a communication problem with the Myriad RF board. Here are hints when software communication check fails:

- If the system test has returned 00 or FF instead of OK then shut down Zipper software and disconnect the Zipper board. Leave for a few seconds before connecting the board and opening the Zipper software again. Start registers test process again.

- If the system returns 00 then there is a problem with the connection between the PC and the board USB port. You will need to check connection and start the process again.

- If the system test returns FF then you know the PC and the USB port are communicating properly. Connect the Zipper board to +5V supply and start the process again. If you now get an OK for the register test map results then the system is ready for testing. If the system still returns 00 or FF instead of an OK, reboot entire connected system starting with the PC.

After the PC has finished rebooting apply power to the Zipper board and restart registers testing.

You should now see the correct OK message and theLMS6002 chip version will be displayed at the bottom left corner of the main window. The system is now ready to commence testing.

3.5 Zipper software description

This section describes the Zipper software tool and each of the buttons and embedded controls. Most of the pages in the tool can be read across to the top level sections of the SPI programming map, with the exception of the 'System page' and the 'ADF4002' page.

The Zipper software consists of several parts: menu bar and toolbar panel, configuration panel, log panel. See panel. See

Figure 12.

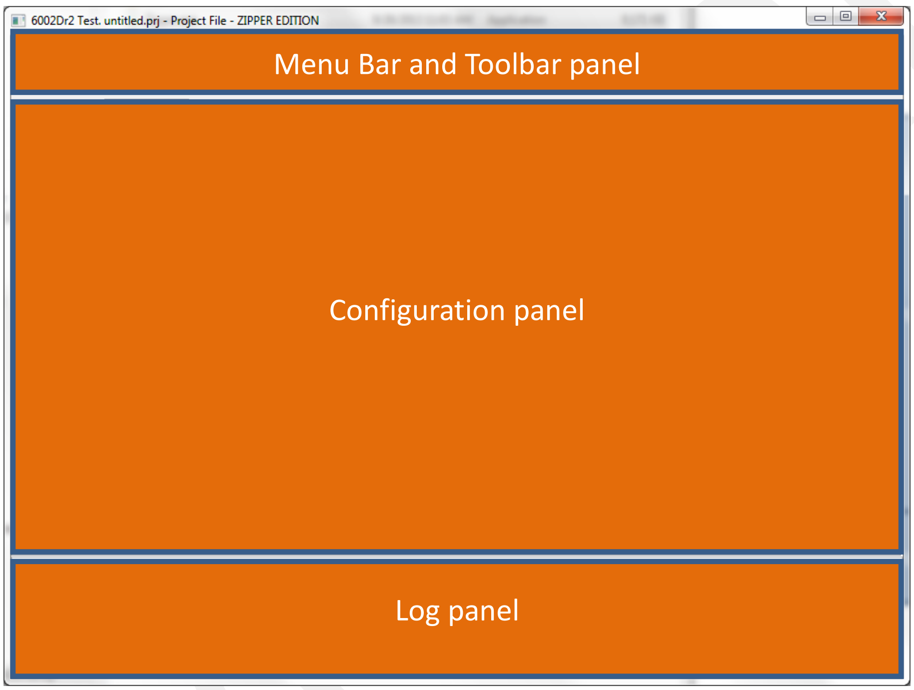


Figure 12. Zipper software window sections.

The **Menu Bar and Toolbar panel** includes basic application configurations. User can start new or save the project with all register settings for LMS6002D chip. The same project file can be loaded using "Open project" command in File menu. Register settings can save to HEX format using "Save to HEX" command.

Configuration panel controls LMS6002D register depending on selected tab.

Log panel logs data of all executed application commands. In the lower left corner shows the LMS6002D chip version.

3.5.1. System Interface

The System interface page allows configuring the synthesizers to the 3GPP bands by channel number and has buttons for bottom, middle and top frequencies for each. This makes changing frequency for the commonly used test channels simpler.

Automatic calibration (the calibrations the device carries out itself under SPI prompting) is also done from this page.

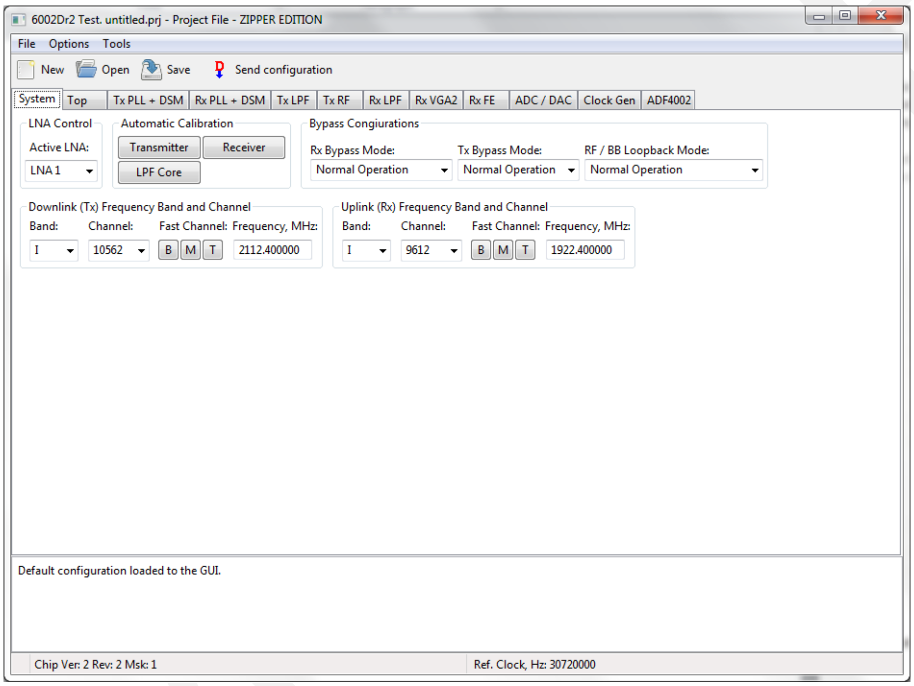


Figure 13. Zipper software System window.

<u>Downlink and Uplink Frequency setting by band/channel number.</u>
The synthesizers can be configured by channel number to the correct frequency in each 3GPP band. Buttons are provided for bottom, middle and top frequencies for each band. This makes changing frequency for the commonly used test channels easier.

<u>Bypass configurations</u>
The various bypass test modes and loop back test modes can be implemented by selecting from the drop down boxes, default is Normal operation.

Automatic Calibration

The Automatic calibration buttons can be used to run through the series of SPI commands required to implement the various self-calibration routines provided on the chip. Use of these macros is implemented as part of a calibration procedure and each button does not carry out a full calibration, use of the buttons in the wrong context could make the calibration state worse rather than better.

Automatic calibration should be done in the following order:

a. LPF Core – Press LPF core button

Executes the process related resistor capacitor (RC) calibration. LPF Core calibration is performed once per device to ensure that the corner frequencies of the LPFs are optimized. The calibration selects the LPF response which is closest and above the required bandwidth. This ensures modulation quality is not adversely impacted but sufficient rejection is provided for adjacent and alternate channel attenuation.

This should be done 1^{st} as optimum DC calibration values for LPF's will change if this is done after the filter DC calibration.

b. Transmitter

The transmitter calibration executes a DC calibration on the TX LPF (I and Q) circuit. This makes the DC contribution at output of filters zero so that DC level at the mixer input does not change when the TX VGA1 gain is changed.

When executing this calibration make sure that no signal is applied to the transmit path. For better DC calibration low DC level signal can applied from baseband via DAC's to transmit path.

c. Receiver

Executes a DC calibration on the Rx LPF (I and Q), and Rx VGA2 (I and Q). This minimizes the DC contribution at output of filters and Rx VGA2.
When executing this calibration make sure that there is no signal applied to Rx input.

3.5.2. Top level

Various loop back and calibrations are also controlled on this page. They are not needed for basic operation. Automatic calibrations should all be done from the 'System' page where macros have been written to apply the calibration routines automatically.

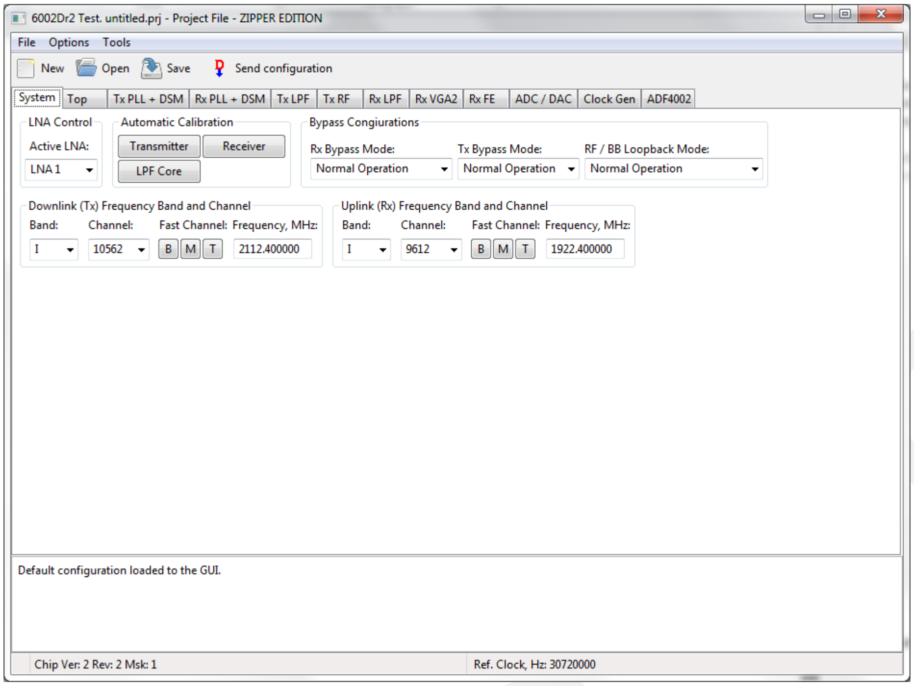


Figure 14. Zipper software Top Level window

Description of each function available from this page is as follows:

DC Calibration

Carries out the top level DC calibration for the device, this is the R component of the RC cal value which is used in each of the LPF (Tx and Rx) process calibration values. Only calibration module address 0 is used.

Clock Buffers control

Enable pins turn the internal clock buffers on and off. These should be enabled when control of the device is needed, however during operation SPI clocks which are not being used should be disabled to reduce the risk of SPI clock spurious.

RF Loopback Control

Test mode. RF loopback control sets the path used for the loopback from Tx to Rx input. Please refer to the SPI programming and calibration document for further details.

BB Loopback Control

Test modes, sets the BB loopback from Tx to Rx input.

Power Control

Soft turn off of Tx and Rx top level blocks of the LMS6002D via SPI. The LMS6002D communication can be easily checked by toggling the “Soft Tx Enable” and “Soft Rx Enable” in the Power Control section. The current change can be observed on power supply.

TRX LPF Calibration

This section is used to calibrate the capacitance of the device to ensure the LPF BW's are correct. To execute the calibration, check then uncheck the reset LPFCAL box (to reset calibration module). Then, check and uncheck the Enable LPFCAL box to execute the calibration. The result can be found in the DC calibration area when the read button is pressed.

Enable Enforce Mode and LPFCAL Code are not used. LPF BW sets the bandwidth used for the calibration. If you are using WCDMA select 2.5MHz. The result should be copied into the TXLPF and RXLPF from 'TRX_LPF_CAL' drop down box.

Decoding

Select 'Decode Signals' or 'Direct Signals' for control of different parts of the SPI memory map. Use 'Decode Signals'.

SPI Port Mode

Selects 3 or 4 wire SPI mode. 4 wire mode is used with the USB board solution.

Rx Bypass Mode

Not used.

DSM Soft Reset

Keep on inactive.

Global Reset

Toggles the reset pin via the USB SPI interface. The LMS6002D should be reset after power up to put it in a known state.

Rx Out/ADC In Switch

Select Closed to monitor receiver analog input. Select Open to route external signal to ADC.

3.5.3. TX PLL + DSM

The Tx PLL is controlled from this page. If the frequency control on the ‘System Interface’ page is used and the correct ‘set up files’ have been automatically downloaded, then this page should not be needed. However a few points to check are that the tick boxes shown in the diagram below are enabled:

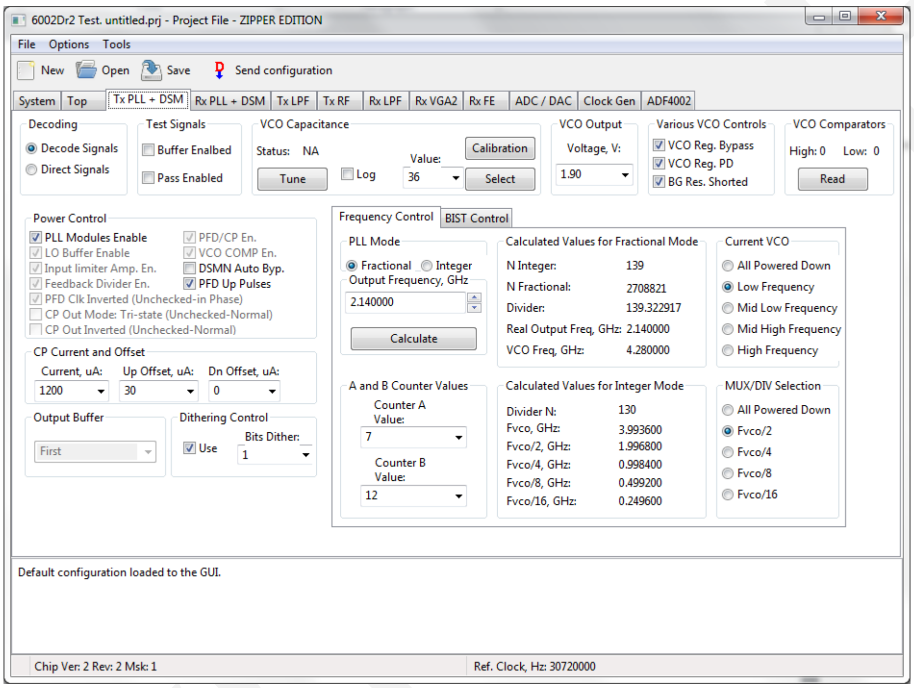


Figure 15. Zipper software TxPLL + DSM window

Description of each function available from this page is as follows:

Decoding
Select ‘Decode’ or ‘Direct’ signals for control of different parts of the SPI memory map. When swapping between the two options the available options are highlighted (and the unavailable ones grayed out). Use ‘Decode’ mode.

Dithering Control
DSM dithering. Leave it set to 1.

Power Control
Individual parts of the PLL circuitry can be turned on and off – leave as default.

Test Signal
Design test signals – leave unchecked.

VCO Comparators
Reads the state of the VCO Comparators. Truth table is:

VTUNE_H	VTUNE_L	Status
0	0	ok
1	0	Vtune is high (> 2.5V) PLL lock not guaranteed.
0	1	Vtune is Low (< 0.5V) PLL lock not guaranteed.
1	1	Not possible, check SPI connections.

Table 1 Comparator readings

Output Buffer
Control not used in TxPLL.

Frequency Control
Sets the PLL divide ratios, VCO and output divider selection. The individual parts of this block are described in more detail below:

PLL Mode
Selects fractional or integer mode. Use fractional mode.

Output Frequency (GHz) - set the desired Tx LO frequency in the text box.
'Calculate' button – calculates the required divide ratio based on the required LO frequency and reference frequency.

To properly select the **'VCO Capacitance'** click "**Tune**" after **"Calculate"**. If you want to observe the VCO capacitor selection algorithm results select "**Log**"

The '**Current VCO**' and the '**MUX/DIV Selection**' show the choice made by pressing **"Calculate"** or **"Tune"** buttons, see below.

VCO Capacitance
Correct setting of VCO capacitance is described in LMS6002D Programming and Calibration Guide**.** Selections made when using the **'Calculate'** button however are decided based on the calibration table used in this block.

To properly select the **'VCO Capacitance'** click "**Tune**" after **"Calculate"**. If you want to observe the VCO capacitor selection algorithm results select "**Log**".

Charge Pump(CP) Current and Offset

CP Current and Offset is set based on the selected loop filter and loop BW. For the recommended loop filter (implemented on the evaluation board) Current should be 1200uA and Up Offset 30uA, as shown.

PLL Calibration Data and File

Press the '**Calibration**' button to enter the Frequency vs Capacitance calibration table data.

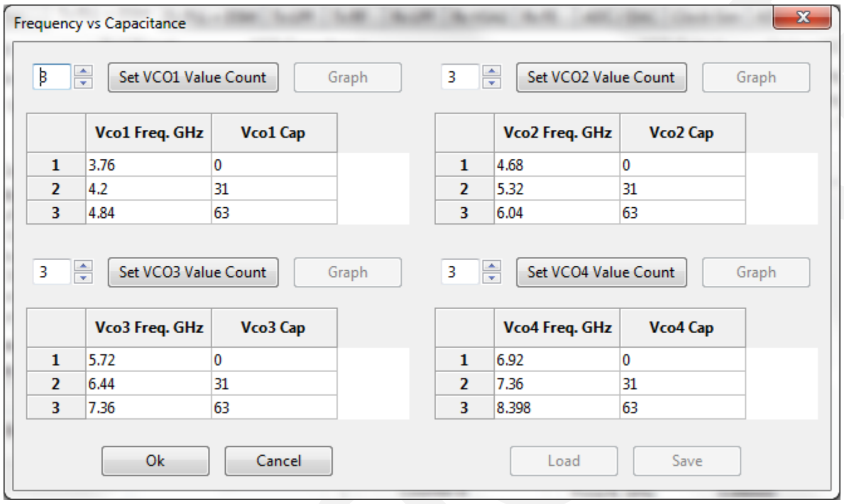


Figure 16. Frequency versus capacitance calibration table data

The calibration data consists of frequency versus capacitance value responses which are defined by minimum 2 point definition. The software automatically gives optimum VCO data. To load a new VCO file press the 'Load' button and follow the normal windows procedure to load a file. Then press OK. This new file will now be downloaded on subsequent starts of the software.

3.5.4. Rx PLL + DSM

The Rx PLL is controlled from this page, if the frequency control on the 'System Interface' page is used and the correct 'set up files' have been automatically downloaded, then this page should not be needed. However a few points to check are that the tick boxes shown in the diagram below are enabled.

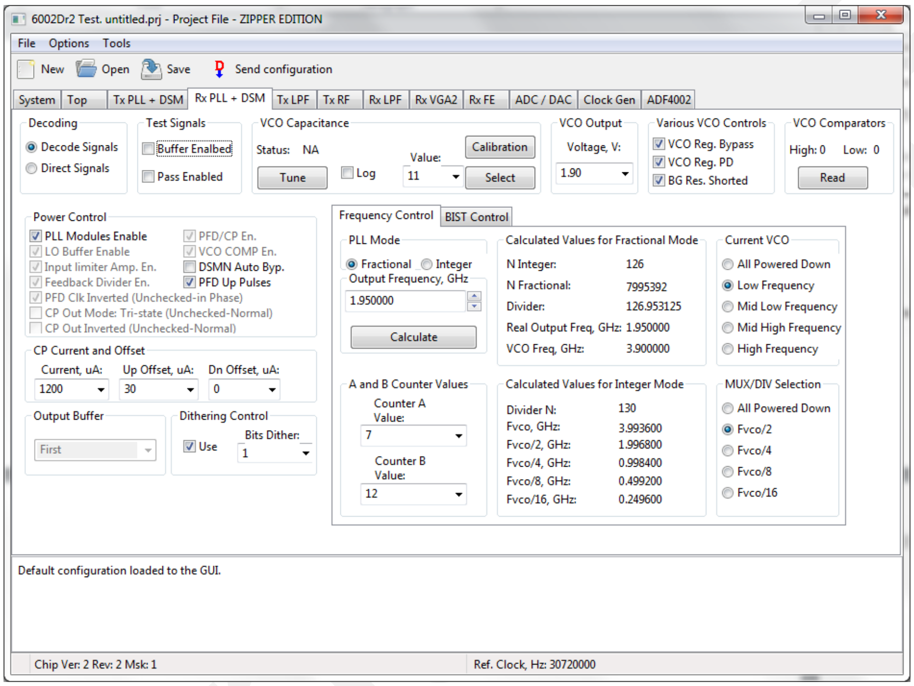


Figure 17. RX PLL + DSM window

Description of each function available from this page is as follows:

<u>Decoding</u>
Select 'Decode' or 'Direct' signals for control of different parts of the SPI memory map. When swapping between the two options the available options are highlighted (and the unavailable ones grayed out). Use 'Decode' mode.

<u>Dithering Control</u>
DSM dithering. Leave it set to 1.

<u>Power Control</u>
Individual parts of the PLL circuitry can be turned on and off – leave as default.

<u>Test Signal</u>
Design test signals – leave unchecked.

VCO Comparators
Reads the state of the VCO Comparators. Truth table is:

VTUNE_H	VTUNE_L	Status
0	0	ok
1	0	Vtune is high (> 2.5V), PLL lock not guaranteed.
0	1	Vtune is Low (< 0.5V), PLL lock not guaranteed.
1	1	Not possible, check SPI connections.

Table 2 Comparator readings

Output Buffer
Sets the correct PLL output buffer for the selected LNA:
LNA 1 = First
LNA 2 = Second
LNA 3 = Third and
Disable.

Selection of LNA in tool on ‘System’ page automatically selects the correct buffer.

Frequency Control
Sets the PLL divide ratios, VCO and output divider selection. The individual parts of this block are described in more detail below.

PLL Mode
Selects fractional or integer mode. Use fractional mode.

Output Frequency (GHz) - set the desired Tx LO frequency in the text box.
‘Calculate’ button – calculates the required divide ratio based on the required LO frequency and reference frequency.

To properly select the **‘VCO Capacitance’** click “**Tune**” after **“Calculate”**. If you want to observe the VCO capacitor selection algorithm results select “**Log**”.

The ‘**Current VCO**’ and the ‘**MUX/DIV Selection**’ show the choice made by pressing **“Calculate”** or **“Tune”** buttons, see below.

VCO Capacitance
Correct setting of VCO capacitance is described in LMS6002D Programming and Calibration Guide**.** Selections made when using the **‘Calculate’** button however are decided based on the calibration table used in this block.

To properly select the **‘VCO Capacitance’** click “**Tune**” after **“Calculate”**. If you want to observe the VCO capacitor selection algorithm results select “**Log**”.

Charge Pump(CP) Current and Offset

CP Current and Offset is set based on the selected loop filter and loop BW. For the recommended loop filter (implemented on the evaluation board). Current should be 1200uA and Up Offset 30uA, as shown.

PLL Calibration Data and File

Press the **'Calibration'** button to enter the Frequency vs Capacitance calibration table data.

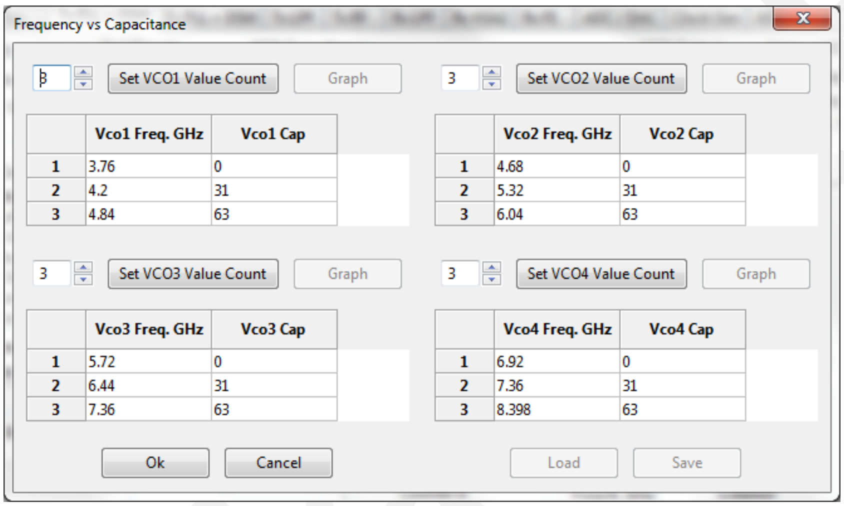


Figure 18. Frequency vs capacitance calibration table data

The calibration data consists of frequency versus capacitance value responses which are defined by minimum 2 point definition. The software automatically gives optimum VCO data. To load a new VCO file press the 'Load' button and follow the normal windows procedure to load a file. Then press OK. This new file will now be downloaded on subsequent starts of the software.

3.5.5. Tx LPF

The Tx LPF page contains the SPI controls for the transmitter low pass filters, notably the LPF BW and also the controls for the DC calibration.

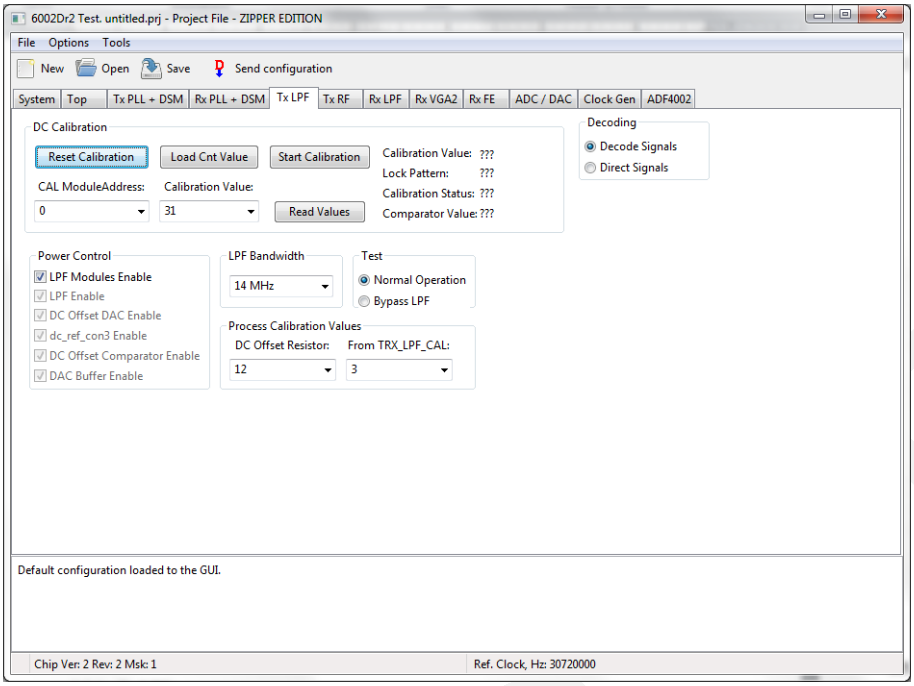


Figure 19. Tx LPF window

Description of each function available from this page is as follows:

DC Calibration
These are the individual controls for the DC correction and auto-calibration routines for the TX LPF (controlled by the 'Transmitter' auto-calibration button on the 'System' page).

The Tx LPF DC calibration has 2 stages which can be calibrated:

- TXLPF(I) at Cal module address 0
- TXLPF(Q) at Cal module address 1

Power Control
Powers down the LPF modules, grayed out controls can be accessed by using direct signals mode.

LPF Bandwidth
Set the LPF BW in the drop down box, from 0.75MHz to 14MHz. Note RF system BW is twice this number, i.e. 0.75MHz LPF BW is 1.5MHz system BW.

Test
Enables LPF bypass for test purposes. Ensure 'Normal Operation' is enabled.

Process Calibration Values
RC calibration values used to process trim the LPF BW. Values are calculated in top level calibration and written into these locations (carried out automatically by ‘LPF Core’ on ‘System’ page).

Decoding
Select ‘Decode’ or ‘Direct’ signals for control of different parts of SPI memory map. When swapping between the 2 options the available options are highlighted (and the unavailable ones are grayed out). ‘Decode’ mode is recommended.

3.5.6. Tx RF

The TX RF page contains the SPI controls for the TX RF stages, including all Tx gain control, LO correction and Tx output selection.

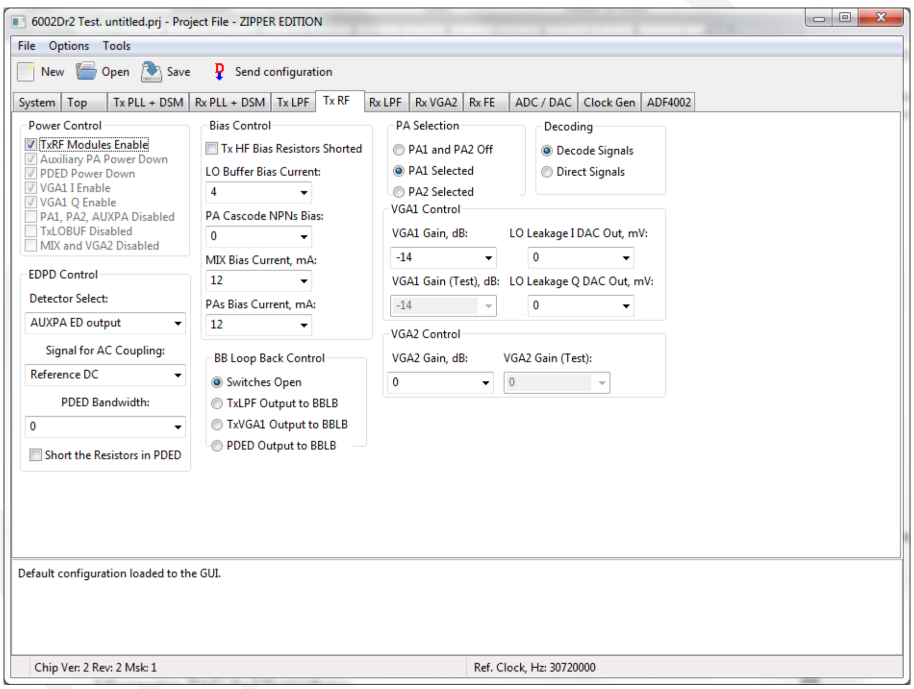


Figure 20. Tx RF window

Description of each function available from this page is as follows:

Power Control
Powers down stages within the Tx RF block – grayed out controls are accessible via ‘Direct’ decoding mode.

Decoding
Select 'Decode' or 'Direct' signals for control of different parts of SPI memory map. When swapping between the 2 options the available options are highlighted (and the unavailable ones grayed out). 'Decode' mode is recommended.

VGA1 Control
VGA1 Gain sets VGA1 gain (IF gain stage) from -4 to -36dB via drop down box. VGA1 Gain (Test) sets VGA1 gain in 'Direct Signals' mode by setting 8 bit not log-linear control word directly. 'LO Leakage I DAC Out' and 'LO Leakage Q DAC Out' set DC level injected via the LO correction DACs for LO cancellation.

VGA2 Control
VGA2 Gain sets VGA2 gain (RF gain stage) from 0 to 25dB via drop down box. VGA2 Gain (Test) set VGA2 gain in 'Direct Signals' mode by setting 9 bit not log-linear control word directly.

PA Selection
Select Tx output stage PA1, PA2 or both off.

3.5.7. Rx LPF

The Rx LPF page contains the SPI controls for the receiver low pass filters, notably the LPF BW and also the controls for the DC calibration.

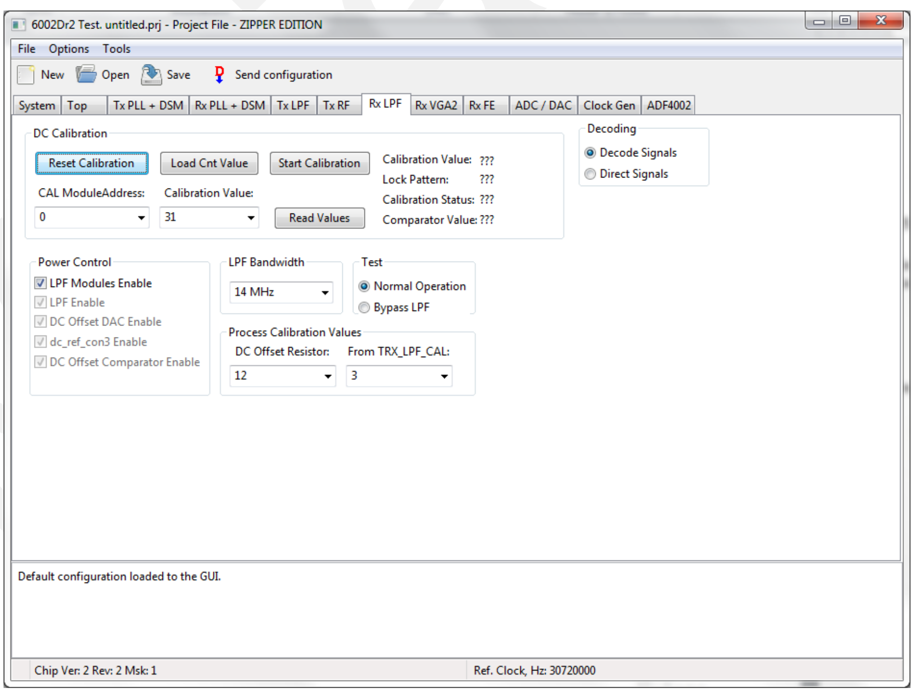


Figure 21. Rx LPF window

Description of each function available from this page is as follows:

DC Calibration
These are the individual controls for the DC correction and auto-calibration routines for the RX LPF (controlled by the 'Receiver' auto-calibration button on the 'System' page).
The Rx LPF DC calibration has 2 stages which can be calibrated:

- RXLPF(I) at Cal module address 0
- RXLPF(Q) at Cal module address 1

Power Control
Powers down the LPF modules, grayed out controls can be accessed by using direct signals mode. Using 'Decode' mode is recommended.

LPF Bandwidth
Set the LPF BW in the drop down box, from 0.75MHz to 14MHz. Note that RF system BW is twice this number, i.e. 0.75MHz LPF BW is 1.5MHz system BW.

Test
LPF bypass for test purposes. Ensure 'Normal Operation' is enabled.

Process Calibration Values
RC calibration values used to process trim the LPF BW, values are calculated in top level calibration and written into these locations (carried out automatically by 'LPF Cal' on 'System' page).

Decoding
Select 'Decode' or 'Direct' signals for control of different parts of the SPI memory map. When swapping between the 2 options the available options are highlighted (and the unavailable ones grayed out).

3.5.8. RX VGA2

SPI controls for the RX VGA2 stage settings.

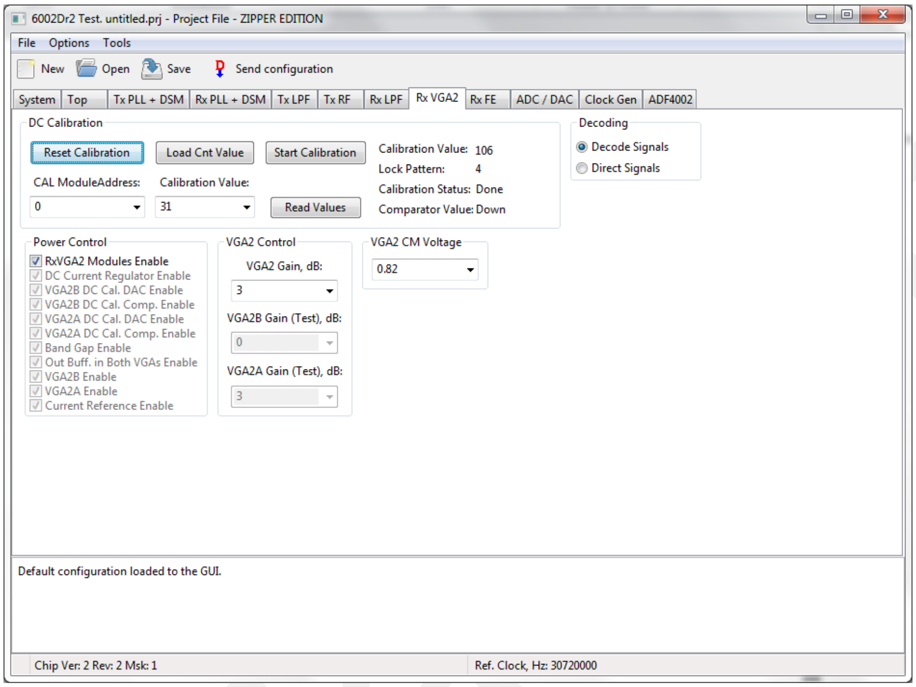


Figure 22. Rx VGA2 window

Description of each function available from this page is as follows:

DC Calibration
These are the individual controls for the DC correction and auto-calibration routines for the RX VGA2 (controlled by the 'Receiver' auto-calibration button on the 'System' page).

The Rx VGA2 DC calibration has 5 stages which can be calibrated:

- RXVGA2 Top at Cal module address 0
- RXVGA2a(I) at Cal module address 1
- RXVGA2a(Q) at Cal module address 2
- RXVGA2b(I) at Cal module address 3
- RXVGA2b(Q) at Cal module address 4

.

Decoding
Select 'Decode' or 'Direct' signals for control of different parts of SPI memory map. When swapping between the 2 options the available options are highlighted (and the unavailable ones grayed out). Use 'Decode' mode.

Power Control

Powers down the RXVGA2 modules, grayed out controls can be accessed by using direct signals mode.

VGA2 Control

Sets RXVGA2 Gain, available range is 0 to 30dB in 3dB steps. Decoding is set to 'Decode Signals' for normal use.

VGA2B Gain (Test) and VGA2A Gain (Test) are available in test mode to control A and B stages directly. Decoding is set to 'Direct Signals' to use this function. This feature is not used for normal operation.

VGA2 CM Voltage

Sets RXVGA2 output common node voltage to interface to ADCs. Code 12, which corresponds to 780mV, is recommended.

3.5.9. RX FE

Sets the SPI controls for the RX Front End stages, including LNA selection, LNA gain, RXVGA1 gain and RX LO cancellation.

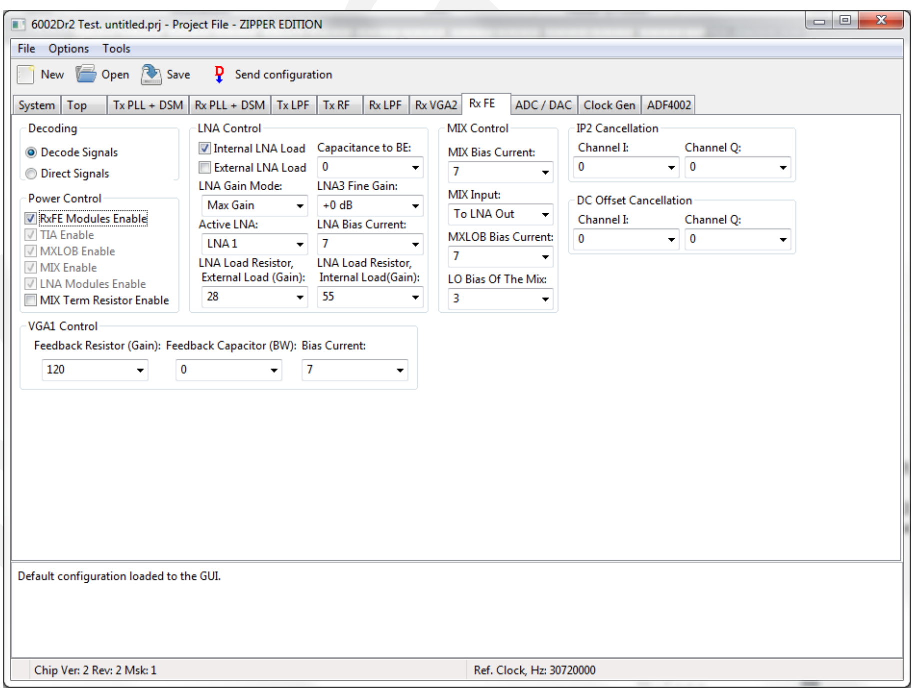


Figure 23. Rx FE window

Description of each function available from this page is as follows:

Decoding
Select 'Decode' or 'Direct' signals for control of different parts of the SPI memory map. When swapping between the 2 options the available options are highlighted (and the unavailable ones grayed out).

Power Control
Powers down the RXFE modules, grayed out controls can be accessed by using direct signals mode.

DC Offset Cancellation
Applies DC level to mixer output to cancel DC level from LO leakage.

IP2 Cancellation
Applies offset to mixer to improve IP2 performance. Not required.

LNA Control
Settings for LNA controls are as follows:

- Internal/External LNA load tick boxes – use internal.
- Capacitance to BE – leave as default (0)
- LNA Gain Mode – selects LNA gain, Max, Mid and Bypass.
- LNA3 Fine Gain – fine gain setting for LNA3 which has no bypass mode, 0 to + 3dB.
- Active LNA – Select active LNA 1 to 3, also need to change the RX LO buffer in 'RX PLL + DSM' page when changing LNA. This control changes RX LO buffer automatically.
- LNA bias current – leave at default (7).
- External load – not used when Internal load selected.
- Internal Load (0 to 63) sets LNA gain, max (0dB) = 55, min (-9.2dB) = 0. Do not set above 55.

MIX Control
Settings for Mix control are shown below, do not change:

- MIX Bias current – '7', leave it at default.
- MIX Input – 'To LNA Out', leave it at default.
- MXLOB Bias Current – '7', leave it at default.
- LO Bias Of The MIX – '3', leave it at default.

VGA1 Control
Feedback Resistor (0 to 123). Only use settings up to 120
Sets VGA1 gain, max (0dB) = 120, min (-24dB) = 0, so do not set above 120. Gain control is not log-linear.

Feedback capacitor (0 to 123)
Introduces a single pole LPF at VGA1 output. Bandwidth dependent on 'Feedback resistor' and 'Feedback capacitor'. For no filtering leave at default (0).

Bias Current - leave at default (7).

3.5.10. ADC/DAC

ADC / DAC page sets all the controls for the data ADCs in the receive path and data DACs in the transmit path.

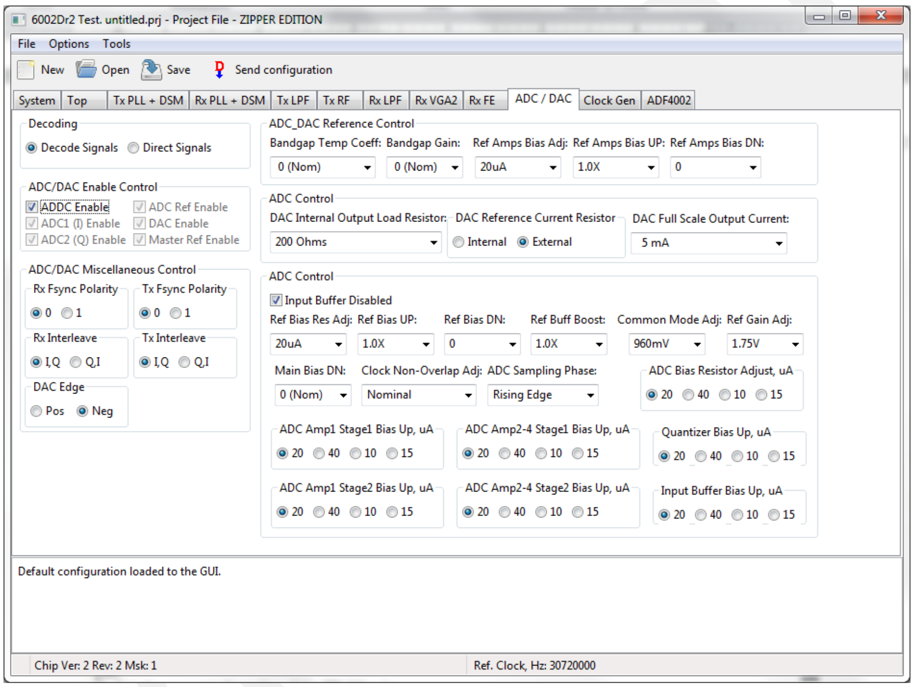


Figure 24. ADC/DAC window

Description of each function available from this page is as follows:

<u>Decoding</u>
Select 'Decode' or 'Direct' signals for control of different parts of the SPI memory map. When swapping between the two options, the available options are highlighted (and the unavailable ones are grayed out).

<u>ADC/DAC Miscellaneous Control</u>
Rx Fsync Polarity – sets the polarity of the RX IQ SEL signal for the first sample of the Rx IQ pair.
Rx Interleave – sets the order of the RX IQ pair.

Tx Fsync Polarity – sets the polarity of the TX IQ SEL signal for the first sample of the Tx IQ pair.
Tx Interleave – sets the order of the TX IQ pair.

See diagram below for explanation:

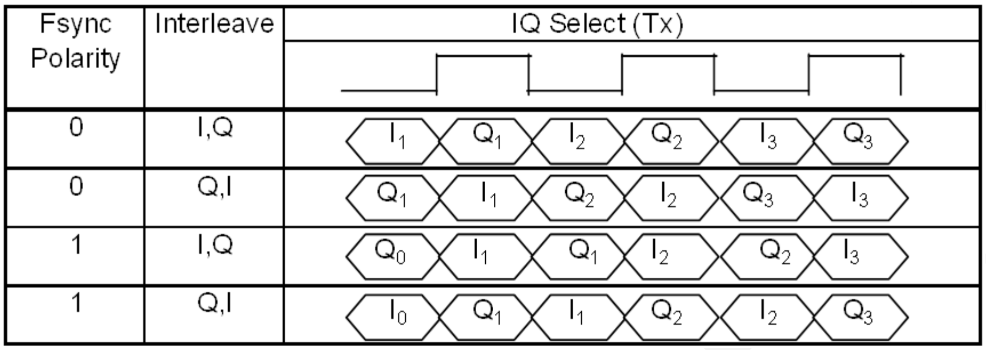


Figure 25. DAC enable control timing for TX

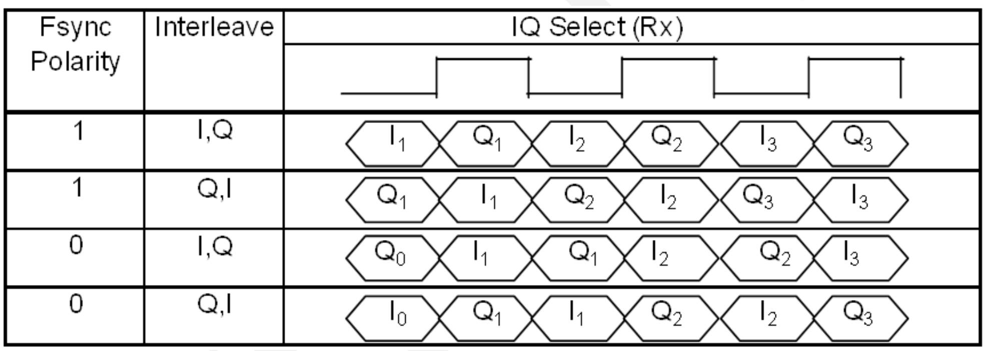


Figure 26. ADC enable control timing for RX

DAC Edge

DAC Edge – selects the edge of the DAC clock which the data is clocked from. Negative is usually required.

ADC/DAC Enable Control

Check 'ADC Enable' to enable ADCs and DACs. Sub-blocks are also independently controllable in 'Direct Signals' mode.

DAC Control

- Internal output Load Resistor 50, 66, 100, 200 Ohms or Open Circuit setting (when using external load resistor).
- DAC Reference Current resistor – use External.

- DAC Full Scale Output Current (2.5, 5, 10mA). Use Load resistor and Full scale output current to control DAC output voltage swing.

ADC/DAC Reference Control
Use default settings:

ADC Control
Use default settings with following exceptions:
Ref Bias Res Adj = 10uA (minimizes ADC noise)
Common mode Adj = 960mV.
Ref Gain Adj = 1.75V.

3.5.11. Clock Gen

This page provides control of on board clock generator which allows user to generate the reference clock to Myriad RF board as well as digital interface.

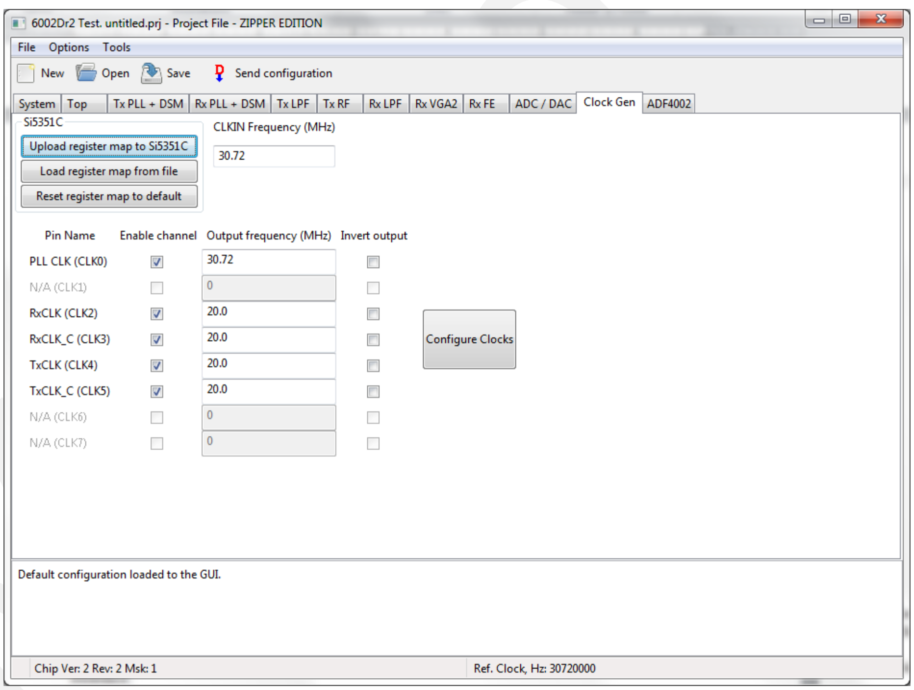


Figure 27. Control window for on board clock generator.

The default settings will program the standard board with a 30.72MHz TCXO to have PLL CLK to 30.72MHz and digital interface to 20 MHz. Please note that with default board configuration the Myriad RF PLL CLK pin is supplied directly from TCXO. With simple boards modification PLL

CLK can be supplied directly from Si5351C clock generator. More information you can find in section **4.5.**

Using this feature:

- Enable clock channel
- Input desired frequency value
- Press "Configure Clocks"
- Press "upload register map to Si5351C"

3.5.12. ADF4002

This page provides the SPI control via a second enable pin on the SPI interface for an external PLL chip. The purpose of this is so the interface TCXO can be locked to external test equipment if required.

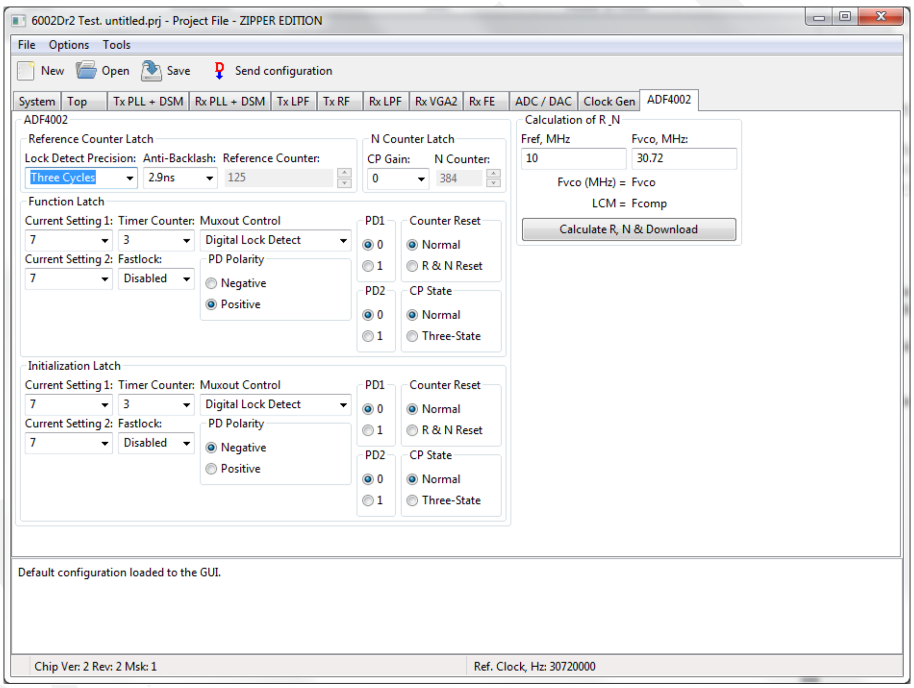


Figure 28. Control window for on board ADF4002.

The default settings will program the standard board with a 30.72MHz TCXO and a 10MHz reference. When 10 MHz reference is connected to board J8 connector, press 'Calculate R,N & Download' button. If all is correct the green PLL locked LED (LD4) on the interface board should illuminate.

4

Development Kit Connections

4.1 Basic Connections

The Myriad-RF board can be used as a standalone board or in conjunction with the Zipper board. The Myriad-RF board is connected to the Zipper board via the standard connector FX10A-80P. The following sections describe the connections on both boards as well as the overall functionality.

4.2 Myriad-RF Board Connections

The analog differential IQ interface is also available on Myriad-RF board and provided via X4 and X5 connectors, see Figure 29. X6 and X7 are the RF connection for receiver input and transmitter output on the RF board, see Figure 29. The RF board is tuned to support band 1 (Tx 2140 MHz and Rx 1950 MHz) and broadband operation. The front end switches are configurable for selected receiver input and transmitter output via GPIO's. The truth table for each selection mode (RX and/or TX) is shown in section 4.7.

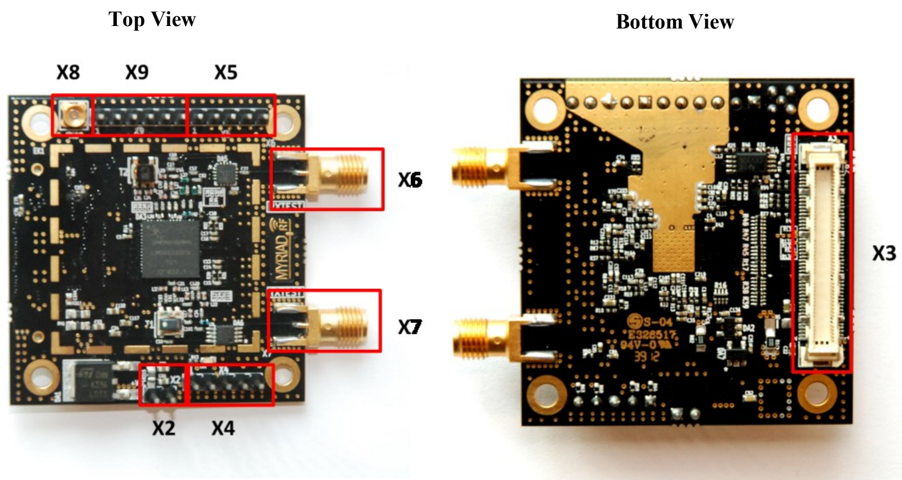


Figure 29. Myriad-RF board connection descriptions.

Myriad-RF board connectors are described in the table below.

Connector	Name	Description
X2	+5 V supply	External +5 V supply.
X3	Digital I/O	The FX10A-80P is a standard connector used to interface the RF board directly to interface board or any other baseband board.
X4	TX Analog I/Q	Connector used to provide or get transmit analog I/Q signals.
X5	RX Analog I/Q	Connector used to measure receiver analog I/Q signals.
X6	RXTEST	SMA connector provides connection to low band or high band RX input. Requires preselected RF switch configuration.
X7	TXTEST	SMA connector that provides connection to low band or high band TX output. Requires preselected RF switch configuration.
X8	Ext – CLK	Connector used to supply PLL clock externally.
X9	Ext – SPI	Connector used to control LMS6002DFN SPI registers externally. SPI registers are usually controlled via X3 connector.

Table 3. Myriad-RF Board Connector Assignments

4.2.1. X2 – +5V Supply Connector

The pin header type connector used to supply +5 V for Myriad-RF board in standalone mode.

4.2.2. X3 – Digital I/O Connector

The Myriad-RF board X3 connector (type FX10A-80P0) is pin compatible with J1 connector on interface board, see Figure 29. It provides the digital and SPI interface for LMS6002DFN together with the supply voltage and GPIO control for RF switches for Myriad-RF board. The pin descriptions on this connector are given in the table below:

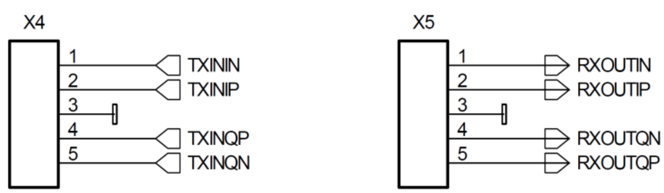
Pin No	Pin Name	Type	Description
1	+5 V	in DC	+5 V power supply
2	+5 V	in DC	+5 V power supply
3	+5 V	in DC	+5 V power supply
4	+5 V	in DC	+5 V power supply
5	GND		Ground pin
6	GND		Ground pin
7	+3.3V	in DC	+3.3 V power supply optional
8	+3.3 V	in DC	+3.3 V power supply optional
9	+3.3V	in DC	+3.3 V power supply optional
10	+3.3V	in DC	+3.3 V power supply optional
11	GND		Ground pin
12	GND		Ground pin
13	-		Not used
14	-		Not used
15	-		Not used
16	-		Not used
17	GND		Ground pin
18	GND		Ground pin
19	TXIQSEL	in cmos	TX digital interface IQ flag
20	-		Not used
21	-		Not used
22	-		Not used
23	TXD0	in cmos	DACs digital input, bit 0 (LSB)
24	TXD1	in cmos	DACs digital input, bit 1
25	TXD2	in cmos	DACs digital input, bit 2
26	TXD3	in cmos	DACs digital input, bit 3
27	GND		Ground pin
28	GND		Ground pin
29	TXD4	in cmos	DACs digital input, bit 4
30	TXD5	in cmos	DACs digital input, bit 5

31	TXD6	in cmos	DACs digital input, bit 6
32	TXD7	in cmos	DACs digital input, bit 7
33	TXD8	in cmos	DACs digital input, bit 8
34	TXD9	in cmos	DACs digital input, bit 9
35	TXD10	in cmos	DACs digital input, bit 10
36	TXD11	in cmos	DACs digital input, bit 11 (MSB)
37	GND		Ground pin
38	GND		Ground pin
39	RXIQSEL	out cmos	RX digital interface IQ flag
40	-		Not used
41	-		Not used
42	-		Not used
43	RXD0	out cmos	ADCs digital output, bit 0 (LSB)
44	RXD1	out cmos	ADCs digital output, bit 1
45	RXD2	out cmos	ADCs digital output, bit 2
46	RXD3	out cmos	ADCs digital output, bit 3
47	GND		Ground pin
48	GND		Ground pin
49	RXD4	out cmos	ADCs digital output, bit 4
50	RXD5	out cmos	ADCs digital output, bit 5
51	RXD6	out cmos	ADCs digital output, bit 6
52	RXD7	out cmos	ADCs digital output, bit 7
53	RXD8	out cmos	ADCs digital output, bit 8
54	RXD9	out cmos	ADCs digital output, bit 9
55	RXD10	out cmos	ADCs digital output, bit 10
56	RXD11	out cmos	ADCs digital output, bit 11 (MSB)
57	GND		Ground pin
58	GND		Ground pin
59	RXCLK	in cmos	RX digital interface clock
60	TXCLK	in cmos	TX digital interface clock
61	-		Not used
62	-		Not used
63	GND		Ground pin
64	GND		Ground pin
65	GPIO0		
66	RESET	in cmos	Hardware reset, active low
67	GPIO1		
68	SPI_MOSI	out cmos	Serial port data out
69	GPIO2		
70	SPI_MISO	in/out cmos	Serial port data in/out
71	-		Not used
72	SPI_CLK	in cmos	Serial port clock, positive edge sensitive

73	GND		Ground pin
74	SPI_NCSO	in cmos	Serial port enable, active low
75	CLK_IN	in cmos	PLL reference clock input
76	-		Not used
77	GND		Ground pin
78	-		Not used
79	TXEN	in cmos	Transmitter enable, active high
80	RXEN	in cmos	Receiver enable, active high
81	GND		Ground pin
82	GND		Ground pin
83	GND		Ground pin
84	GND		Ground pin
85	GND		Ground pin
86	GND		Ground pin
87	GND		Ground pin
88	GND		Ground pin

Table 4 X3 connector pin description

4.2.3. X4 and X5 – Analog IQ Connectors



Pin header type connectors on the Myriad-RF board, provide analog IQ signals I/O.

4.2.4. X6 and X7 – RF Input and Output

The X6 and X7 are SMA type connectors which provide Receive input and Transmit output to the LMS6002DFN, respectively. These are generally used to connect to antenna or test equipment.

4.2.5. X8 – External CLK Connector

The X8 is micro miniature coaxial connector (MMCX8400). It is optional and used to supply external clock in standalone mode.

4.2.6. X9 – External SPI Connector

This is a pin header type connector used for SPI interface to LMS602DFN. This is optional, if the board is used in standalone mode.

4.3 Zipper Board Connections

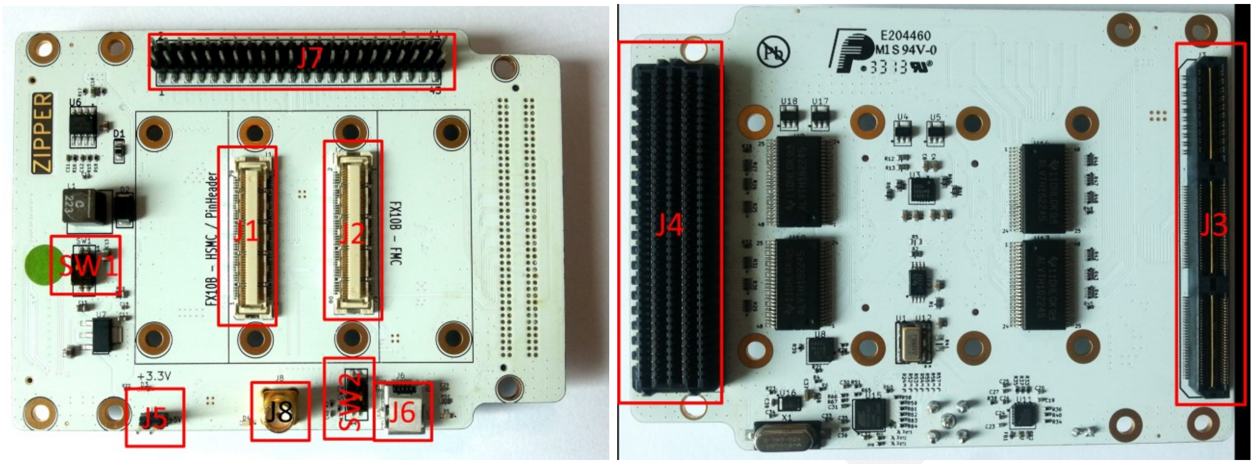


Figure 30. Zipper board connection descriptions.

The following table describes the Zipper board connectors.

Connector	Name	Description
J1	Myriad RF to HSMC and Pinheader	Connects Myriad RF board with HSMC and Pinheader via the FX10A-80P a standard connector.
J2	Myriad RF to FMC and Pinheader	Connects Myriad RF board with FMC via the FX10A-80P a standard connector.
J3	HSMC	HSMC standard Altera development kits connector, connected to all Myriad RF digital inputs/outputs.
J4	FMC	FMC standard Xilinx development kits connector, connected to all Myriad RF digital inputs/outputs.
J5	+5V	+5V input power connector.
J6	MiniUSB	USB connector.
J7	Pinheader	All Myriad RF inputs/outputs are connected.
J8	SMA	Reference clock input for ADF4002 to lock the external clock from test equipment with DigiRED board clock.
SW1	+12V	When switch enabled, Zipper board as well as Myriad RF board can be powered on from +12V voltage supply.
SW2	MCU	A hard reset switch for Atmel MCU

Table 5 Zipper board connectors and switches.

4.3.1. J1 and J2 – Digital I/O Connectors

The Myriad-RF board is directly plugged into one of the FX10A-80P type connectors. The digital I/Q connector is a digital transmit (TX) and receive (RX) interface to the ADC/DAC of the LMS6002D.

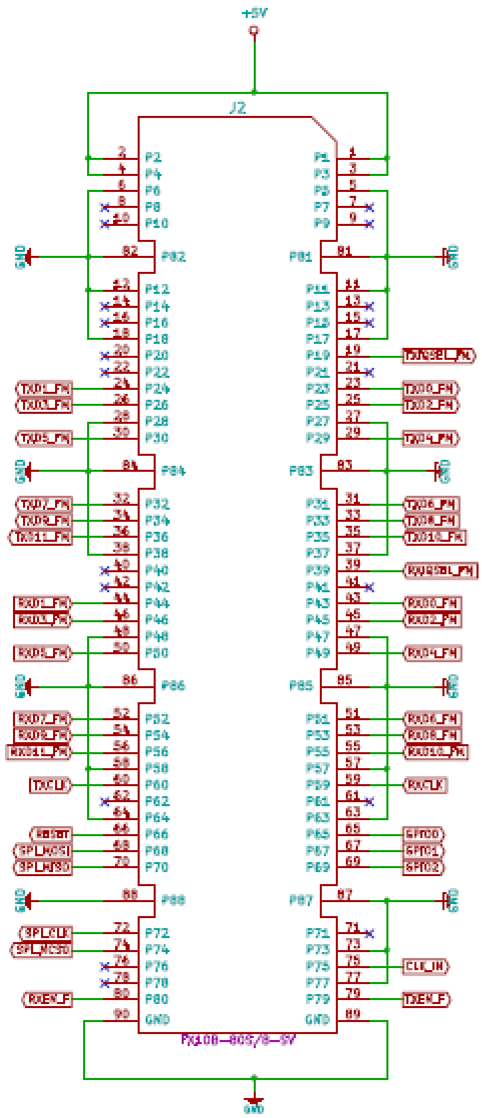


Figure 31. Digital I/O connector

The SPI interface for LMS6002D can also be established via J1 and J2 connector.

4.4 Hardware options: Clocking, SPI, GPIO truth table.

This section describes the configurations and set up procedures for:

- Reference frequency and data clocks distribution (Section 4.5).
- SPI interface configuration (Section 4.6).
- GPIO control truth table (Section 4.7).

The board is shipped in a default mode for basic operation. Various options are available depending on the system configuration required for testing or development work. The options are summarized below and the following sections describe the board modifications required to achieve these configurations.

4.5 Reference Frequency and Data Clocks Distribution

The Myriad RF provides a flexible clocking scheme which enables the PLL clock, RX clock and TX clock to be independently set.

The Zipper board is shipped with a default mode using the on board 30.72MHz clock for PLL clock only. The board can be reconfigured to allow users to provide clock frequency for digital interface and PLL clock using programmable clock generator from Silicon Labs (Si5351C) which is capable of synthesizing four independent frequencies. The device outputs are connected independently to LMS6002D PLL clock, Rx data interface clock and Tx data interface clock.

In order to reprogram the LMS6002D PLL frequency from the default setting of 30.72 MHz, please use component change as given in the table below. Please note that NF denotes that component is not fitted:

Reference clock options		
Description / Component	Default mode. PLL clock set to 30.72 MHz	Programmable mode. PLL clock can be reprogramed.
R2	0 Ohm	NF
R5	NF	0 Ohm

Table 6. Reference clock configurations

4.6 SPI Options

Zipper board offer two options for the SPI communication with Myriad RF board:

1. SPI communication established via USB interface.
2. SPI communication established via J3, J4 or J7 connectors.

In order to make sure stable SPI communication for desired option, the component change on interface board is given in a table below. Please note that NF denotes that component is not fitted:

SPI Options				
SPI Line	**Components**	**SPI via USB**	**SPI via J2, J4 or J7**	**Description**
RESET	R60	0 Ohm	NF	
	R24	NF	0 Ohm	
SPI_MOSI	R62	0 Ohm	NF	
	R55	NF	0 Ohm	
SPI_MISO	R61	0 Ohm	NF	
	R54	NF	0 Ohm	
SPI_SCLK	R63	0 Ohm	NF	
	R56	NF	0 Ohm	
SPI_NCS0	R64	0 Ohm	NF	
	R57	NF	0 Ohm	
SPI_NCS_1	R59	0 Ohm	NF	Master enable for ADF4002 SPI interface
	R53	NF	0 Ohm	
SPI_NCS_2	R58	0 Ohm	NF	Master enable for Si5351 SPI interface
	R52	NF	0 Ohm	
GPIO 0	R68	0 Ohm	NF	GPIO for RF switch, controlled via GUI.
	R71	NF	0 Ohm	
GPIO 1	R69	0 Ohm	NF	GPIO for RF switch, controlled via GUI.
	R72	NF	0 Ohm	
GPIO 2	R70	0 Ohm	NF	GPIO for RF switch, controlled via GUI.
	R73	NF	0 Ohm	

Table 7. SPI configuration table

By default is SPI control is preconfigured to controlled from USB.

4.7 GPIO control truth table

The RF switches on the Myriad RF board are controlled via the GPIO 0-2 logic signals. This enables the user to choose RF input/output depending on the operation frequency. The truth table of the GPIO 0-2 settings is shown below.

LMS6002D RF Input/output	**GPIO 0**	**GPIO 1**	**GPIO 2**	**Description**
TX out 1	X	X	0	High band output (1500 – 3800 MHz)
TX out 2	X	X	1	Broadband output
Rx in 1	1	1	X	Low band input (300 – 2200 MHz)
Rx in 2	0	1	X	High band input (1500-3800MHz)
Rx in 3	0	0	X	Broadband input

Table 8. GPIO truth table